

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today
(1) was not written for publication in a law journal and
(2) is not binding precedent of the Board.

Paper No. 18

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HENRY W. ADAMS, III,
THOMAS B. GENDUSO, and WAN L. LEUNG

Appeal No. 1998-1510
Application 08/205,737

ON BRIEF

Before KRASS, FLEMING, and DIXON, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of
claims 1 through 5, all of the claims remaining in the
application.

Appeal No. 1998-1510
Application No. 08/205,737

The invention is directed to a method of cache memory storage space management.

Independent claim 1 is reproduced as follows:

1. A method of managing POP read data information contained in a stack cache memory device, in a computer system having a main memory and a processor associated with the stack cache memory device, said stack cache memory device including at least one cache line containing a plurality of words having adjacent address locations, said address locations arranged from a lowest address to a highest address within said at least one cache line, said method comprising the steps of:

(i) initiating a POP read operation with said processor to read data;

(ii) determining if said read data is contained within said stack cache memory device;

(iii) determining if said read data corresponds to the highest address word in said at least one cache line; and

(iv)(a) passing said read data from said stack cache memory device to said processor and invalidating all of said plurality of address locations in said at least one cache line if said read data is contained within said stack cache memory device and said read data corresponds to the highest address word in said at least one cache line; or

(iv)(b) directing said processor to retrieve said read data from said main memory without copying said read data to said at least one cache line if said read data is not contained within said stack cache memory device and said read data corresponds to the highest address word in said at least one cache line; else

Appeal No. 1998-1510
Application No. 08/205,737

(iv)(c) not invalidating said at least one cache line if said read data does not correspond to the highest address word in said at least one cache line.

The examiner relies on the following references:

Chang et al. (Chang) 1980	4,197,580	Apr. 8,
Baum et al. (Baum) 1990	4,928,239	May 22,

Intel, "386™ DX Microprocessor Programmer's Reference Manual" (1991).

Claims 1 through 5 stand rejected under 35 U.S.C. § 103 as unpatentable over Intel in view of Baum.

Reference is made to the briefs and answer for the respective positions of appellants and the examiner.

OPINION

Claims 1 through 5 will stand or fall together, as indicated by appellants at page 6 of the principal brief. Accordingly, we will limit our consideration to the rejection of independent claim 1.

The examiner's position is that Intel discloses the claimed subject matter except that the cache used by Intel does not invalidate the line if the word being referenced in the cache line is the highest addressed. The examiner then relies on Baum for the teaching of invalidating a line in a cache when a POP instruction has been issued and that POP

Appeal No. 1998-1510
Application No. 08/205,737

instruction is loading the last data word from that line for the purpose of eliminating an unnecessary storeback for that cache line and immediately making available for new data a line in the cache that is no longer needed. Thus, concludes the examiner, it would have been obvious to modify Intel to invalidate a cache line when it is known that the cache line will not be accessed again because the POP operation has removed the last word from that cache line.

However, paragraph (iv)(b) of claim 1 requires the step of

directing said processor to retrieve said read data from said main memory without copying said read data to said at least one cache line if said read data is not contained within said stack cache memory device and said read data corresponds to the highest address word in said at least one cache line...

Thus, when there is a cache MISS on a POP read and the read data corresponds to the highest address word, the instant invention causes the processor to retrieve the read data from the main memory without copying the read data to the cache line. Neither Intel nor Baum addresses such a situation. We agree with appellants that while Baum may describe certain stack cache operations when there is a POP to the last word in a cache line and there is a cache HIT, Baum is completely

Appeal No. 1998-1510
Application No. 08/205,737

silent on stack cache operations when there is a POP read to the last word in the cache line and there is a cache MISS [principal brief-page 10]. The examiner does not deny that neither Intel nor Baum discloses the claimed limitation of retrieving data from the main memory without copying the read data to the cache line if the read data is not contained within the stack cache memory and the read data corresponds to the highest address word in the cache line. The examiner merely attempts to explain away this difference.

From the bottom of page 4 to the first line of page 5 of the answer, the examiner contends that the artisan would know that if there is a MISS in the cache and the data being accessed is the highest addressed, there is no need in storing the data in the cache and one would bypass the cache and provide the data directly to the CPU, preventing unnecessary data from being stored in the cache memory. Since neither Intel nor Baum suggests this, it appears to us that the examiner is relying on impermissible hindsight in reaching this conclusion.

In order to buttress his position, the examiner explains, at pages 5-8 of the answer, with the use of drawings attached

Appeal No. 1998-1510
Application No. 08/205,737

as an appendix to the answer, that while step (iv)(b) of instant claim 1 is not actually taught by Intel or Baum, this claimed step is "believed to be one of logical reasoning and/or common sense." Basically, the examiner shows why certain operations would result in inefficiencies and then concludes [answer-page 7] that the "most obvious way" of eliminating those inefficiencies would be "to not load the entire cache line into the cache." While a claimed invention may seem simple and merely the result of "logical reasoning and/or common sense" in retrospect, i.e., after an applicant discloses the invention, the examiner must still show some evidence in the prior art or present a cogent line of reasoning as to why the claimed subject matter would have been obvious to the skilled artisan at the time of the invention. We are not convinced by the examiner's line of reasoning as it appears that the examiner's conclusion would have been obvious to "not load the entire cache line into the cache" in a cache MISS situation where the data being accessed as the highest addressed is based on appellants' own disclosure.

The examiner attempts to bring in a reference to Chang for the concept of not storing data into the cache memory upon

Appeal No. 1998-1510
Application No. 08/205,737

a cache MISS. However, Chang forms no part of the instant statement of rejection and we will not consider this reference in our decision. Where a reference is relied on to support a rejection, whether or not in a minor capacity, there would appear to be no excuse for not positively including the reference in the statement of rejection. In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970).

If the examiner wishes to re-open prosecution, applying Chang against the instant claims, the examiner should bear in mind appellants' arguments in the reply brief and be prepared to answer the argument that Chang invalidates single words in a cache memory rather than invalidating data based on read data corresponding to the highest address word in a multi-word cache line and a cache MISS.

The examiner's decision rejecting claims 1 through 5 under 35 U.S.C. § 103 is reversed.

REVERSED

Errol A. Krass)
Administrative Patent Judge)
)
)
)

Appeal No. 1998-1510
Application No. 08/205,737

PATENT	Michael R. Fleming) BOARD OF
	Administrative Patent Judge) APPEALS AND
) INTERFERENCES
)
)
	Joseph L. Dixon)
	Administrative Patent Judge)

tdl

Appeal No. 1998-1510
Application No. 08/205,737

IBM Corporation, Personal Computer Company
Legal Department 9CCA, Bldg. 205/2
P.O. Box 12195
Research Triangle Park
Raleigh, NC 27709