

THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 16

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN M. CALLAHAN

Appeal No. 1998-1750
Application No. 08/579,490

ON BRIEF

Before KRASS, JERRY SMITH and FRAHM, Administrative Patent Judges.

KRASS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the final rejection of claims 1 through 4, all of the claims pending in the application.

The invention is directed to a high voltage detection circuit best illustrated by

Independent claim 1 as reproduced as follows:

1. A voltage detector circuit which discriminates between a high voltage input signal and a lower input voltage without creating an excessive field across the gate oxide of a sensing transistor, comprising:

an input terminal to which is connected a two-level input signal where the input signal has a first voltage level which is a high voltage level greater than a VCC voltage level, and where the input signal has a second level which is a VCC voltage level;

a PMOS transistor having a source terminal and a substrate terminal, both connected to the input terminal, said PMOS transistor having a gate terminal connected to the VCC voltage level, and said PMOS transistor having a drain terminal;

a shunt NMOS transistor having a drain terminal connected to the drain terminal of the PMOS transistor, said NMOS transistor having a source terminal connected to a ground terminal, and said NMOS transistor having a gate terminal connected to the VCC voltage level, wherein the NMOS transistor is turned on to provide a shunt resistance between the drain terminal of the PMOS transistor and ground;

a series-pass NMOS transistor having a drain terminal connected to the drain terminal of the PMOS transistor, having a source terminal, and having a gate terminal always connected to a VCC voltage level, wherein the gate-to-bulk voltage across the PMOS transistor does not exceed $13 \text{ v} - \text{VCC}$.

The examiner relies on the following references:

Ashmore, Jr.	4,862,019	Aug. 29, 1989
Douglas et al. (Douglas)	5,118,968	Jun. 02, 1992
Mahabadi	5,510,735	Apr. 23, 1996
		(Filed Dec. 29, 1994)

Claims 1 through 4 stand rejected under 35 U.S.C. § 103. As evidence of obviousness, the examiner cites Douglas with regard to claims 1 through 3, adding Mahabadi with regard to claim 4.

Reference is made to the brief and answer for the respective positions of appellant and the examiner.

OPINION

We reverse.

While Figure 2 of Douglas does, arguably, show an input terminal, a PMOS transistor and a shunt NMOS transistor, as claimed, even the examiner admits that the reference does not disclose the claimed “series-pass NMOS transistor having a drain terminal connected to the drain terminal of the PMOS transistor, having a source terminal, and having a gate terminal always connected to a VCC voltage level...”

The examiner explains away this claimed difference by citing it as a “design expedient” depending upon a particular environment. The claim language is fairly explicit in the recitation of this “series-pass NMOS transistor” and its specific interconnection with the other claimed elements. It is insufficient for the examiner to dismiss this integral part of the claimed subject matter by calling it merely a “design expedient” and holding that it would have been obvious to place such a transistor before the inverter 46 of Douglas for the purpose of limiting output current.

We find no reason, other than possibly hindsight gleaned from appellant’s disclosure, for making the modification suggested by the examiner. There is absolutely

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no reason, within the four corners of Douglas, for inserting a series-pass transistor before the inverter and connecting the drain to the drain terminal of the PMOS transistor and having a gate terminal always connected to a supply voltage VCC, as claimed.

The examiner's apparent reliance on U.S. Patent 4,862,019 to Ashmore, Jr. for a showing of a series-pass NMOS transistor has not been considered since Ashmore, Jr. forms no part of the statement of the rejection and there would appear to be no excuse for not positively including the reference in the statement of the rejection if it is being relied upon to support the rejection. In re Hoch, 428 F.2d 1341, 1342 n.3, 166 USPQ 406, 407 n.3 (CCPA 1970). We would further note that the mere showing of a series-pass NMOS transistor being well-known does not necessarily lead to the conclusion that it would have been obvious to place such a transistor in the Douglas circuit in the manner claimed.

Since we will not sustain the examiner's rejection of claim 1, or its dependent claims 2 and 3, under 35 U.S.C. § 103 because of a failure to provide a prima facie case of obviousness, we also will not sustain the rejection of claim 4 under 35 U.S.C. § 103 over Douglas in view of Mahabadi since Mahabadi does not provide for the deficiencies of Douglas regarding the claimed series-pass NMOS transistor. Mahabadi was merely cited by the examiner for its showing of a Schmitt trigger circuit.

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CONCLUSION

The decision of the examiner rejecting claims 1 through 4 under 35 U.S.C.

§ 103 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JERRY SMITH)	APPEALS AND
Administrative Patent Judge)	INTERFERENCES
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