The opinion in support of the decision being entered today was not written for publication in a law journal and is not binding precedent of the Board.

Paper No. 24

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte EDWARD ZAGER and GREGORY MATHEWS

Appeal No. 1998-1801
Application No. 08/285,411

ON BRIEF

Before THOMAS, KRASS, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 18-21, which are all the claims remaining in the application.

We reverse.

BACKGROUND

The invention is directed to a computer system having a set associative cache.

Claim 18 is reproduced below.

> 18. A computer system comprising a 2^n way set associative cache memory subsystem (n>0) including a data array and a corresponding address tag array, characterized by (a) the two arrays being physically disposed in a chip boundary crossing manner, and (b) the two arrays being accessed in a sequential manner, when responding to a read access, and yet the two arrays function as a set associative cache memory,
>
> the chip boundary crossing manner comprising placing the address tag array inside a microprocessor chip while placing the data array outside the microprocessor chip in a single memory bank,
>
> the sequential manner comprising accessing the on-chip address tag array first for cache hit/miss determination and for generation of a cache address by combining n address bits with a plurality of set and line denoting address bits in accordance with the results of the cache hit/miss determination, and accessing only one of the 2^n ways of the off-chip data array subsequently using the generated cache address.

The examiner relies on the following reference:

Moussouris et al. (Moussouris)	5,113,406	May 12, 1992 (filed Mar. 9, 1990)

Claims 18-21 stand rejected under 35 U.S.C. § 103 as being unpatentable over Moussouris.

We refer to the Final Rejection (Paper No. 18) and the Examiner's Answer (Paper No. 21) for a statement of the examiner's position and to the Brief (Paper No. 20) and the

Reply Brief (Paper No. 22) for appellants' position with respect to the claims which stand rejected.

OPINION

The examiner bears the initial burden of presenting a prima facie case of unpatentability. If that burden is met, the burden of coming forward with evidence or argument shifts to the applicant. After evidence or argument is submitted by the applicant in response, patentability is determined on the totality of the record, by a preponderance of evidence with due consideration to persuasiveness of argument. In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992).

The Final Rejection refers to the rejection mailed November 13, 1996 (Paper No. 16) for the rationale underlying the standing section 103 rejection over Moussouris. The examiner points to column 1, lines 60 to column 2, line 34 as the pertinent portion of Moussouris with respect to the subject matter of instant claim 18. (See Paper No. 16, page 3.)

Appellants argue, as set forth principally on page 10 of the Brief, that the reference fails to disclose or suggest "placing the address tag array inside a microprocessor chip while placing the data array outside the microprocessor chip," as reflected in the language of claim 18. Appellants also argue in the Brief and Reply Brief that the "sequential manner" in accessing first the address tag array for hit/miss determination and for generation of a

cache address, and accessing only one of the “2n ways” of the data array “subsequently,” distinguishes over the prior art.

As set forth in particular at pages 8, 11, and 12 of the Brief, appellants assert that, in set associative caches in the prior art, tag and data arrays were simultaneously accessed, in opposition to the “sequential manner” as defined in instant claim 18. Appellants further argue that due to the prior art method of accessing set associative caches, the artisan would not have been motivated to place address tag and data arrays across chip boundaries in the manner required by instant claim 18. The examiner responds in the Answer:

> Since the purpose of the tag RAM and the data RAM are very different and since a tag comparison must be made before any determination of the validity of the data can be made, there seems to be little, if any actual expectation that they be treated the same or accessed simultaneously, as argued.

(Answer, page 4.)

Appellants quote the examiner’s statement in the Reply Brief, and refer to a reference of record as establishing that in the prior art the tag RAM and the data RAM of a set associative cache were expected to be accessed simultaneously. (See Reply Brief, page 2.)

The section of Moussouris pointed out in the rejection deals with placing modules making up cache memory architecture in various combinations with respect to chip boundaries. The reference does not disclose, and has not been alleged to disclose, the

claimed combination of placing the address tag array inside a microprocessor chip and the data array outside the chip. As appellants point out, Moussouris teaches that both the tag and data array should be implemented off the CPU chip (see column 2, lines 47-56). However, appellants appear to recognize that in the context of Moussouris' description of the prior art, this is merely a preferred architecture, and Moussouris may be viewed as providing evidence that, in general, chip boundaries may be arbitrarily drawn.

However, appellants' position is that in a "2^n way set associative" cache memory as presently claimed, the artisan's knowledge of the conventional way of accessing the arrays meant that the artisan would not have arrived at the claimed architecture of placing the address tag array inside a microprocessor chip and the data array outside the chip. Doing so would have been, in effect, going against the conventional wisdom.

The portion of Moussouris identified in the rejection does not appear to describe the specifics of a set associative cache, nor the manner of accessing arrays in a set associative cache. The examiner expresses disagreement with the assumption of simultaneous accessing in prior art set associative cache memories. Yet, appellants point to evidence that is argued to support their position, and the examiner has not addressed the evidence.

Therefore, on this record, we conclude that a critical finding upon which the rejection is based has not been established by a preponderance of the evidence. That is, the

examiner has failed to show there was not expectation in the prior art that the address tag RAM and the data RAM in a 2^n way set associative cache be accessed simultaneously.[1]

The examiner further states that "as conceded by appellants, the direct correspondence between disposition and access timing is inherent." (Answer, page 4.) The statement apparently refers to a sentence on page 9 of the Brief: "Note the direct correspondence between manner of disposition and access timing levels is inherent." However, we do not read appellants' "concession" as an admission relating to knowledge that was in the prior art at the time of invention.

Instant claim 18 is specific as to a computer system comprising a "2^n way set associative cache memory subsystem," with the data array and corresponding address tag array being accessed in the defined "sequential manner," and "accessing only one of the 2^n ways of the off-chip data array subsequently using the generated cache address." Claims 19-21, depending from claim 18, incorporate the specific requirements of claim 18. Why the detailed requirements set forth in claim 18 are deemed to have been obvious in view of the prior art has not been satisfactorily explained. The section 103 rejection appears based in part on Moussouris and in part on unfounded assertions regarding the prior art.

[1] The finding is critical to the rejection because it constitutes the Answer's response to appellants' position regarding "decades of prior art practice [which] calls for accessing both arrays simultaneously," in the words of page 3 of the Answer.

The allocation of burdens requires that the USPTO produce the factual basis for its rejection of an application under 35 U.S.C. § § 102 and 103. In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984) (citing In re Warner, 379 F.2d 1011, 1016, 154 USPQ 173, 177 (CCPA 1967)). The one who bears the initial burden of presenting a prima facie case of unpatentability is the examiner. In re Oetiker, 977 F.2d at 1445, 24 USPQ2d at 1444. The reference as applied is not sufficient to establish prima facie obviousness of the claimed subject matter as a whole, in view of appellants' unanswered arguments. We therefore cannot sustain the section 103 rejection of the claims.

CONCLUSION

The rejection of claims 18-21 is reversed.

REVERSED

JAMES D. THOMAS Administrative Patent Judge	)))))) BOARD OF PATENT
ERROL A. KRASS Administrative Patent Judge	) APPEALS) AND) INTERFERENCES)))
HOWARD B. BLANKENSHIP Administrative Patent Judge	))

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