

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte OM P. AGRAWAL,  
BRADLEY A. SHARPE GEISLER,  
and NICHOLAS A. SCHMITZ

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Appeal No. 1999-0133  
Application No. 08/459,570

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ON BRIEF

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Before JERRY SMITH, GROSS, and LEVY, Administrative Patent Judges.  
LEVY, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-28<sup>1</sup>, which are all of the claims pending in this application.

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<sup>1</sup> An amendment (Paper No. 9, filed February 13, 1997) submitted subsequent to the final rejection (Paper No. 6, mailed September 6, 1996) has been entered by the examiner (Paper No. 11, mailed March 3, 1997).

BACKGROUND

Appellants' invention relates to a programmable optimized-distribution logic allocator for a high-density complex programmable logic device (PLD). An understanding of the invention can be derived from a reading of exemplary claim 1, which is reproduced as follows:

1. A method for distributing product terms from a programmable array in a very high-density CPLD to logic in said very high-density CPLD, said method comprising:

coupling each product-term cluster in a plurality of product-term clusters to a different input line of a programmable logic allocator;

configuring said logic allocator so that each output line of said logic allocator has programmable access to a first predetermined number of product-term clusters in said plurality of product-term clusters;

wherein said first predetermined number of product-term clusters includes at least twenty product terms; and

upon programmably connecting a product-term cluster to an output line of said logic allocator, said connected product-term cluster is disconnected from all remaining output lines of said logic allocator.

The prior art reference of record relied upon by the examiner in rejecting the appealed claims is:

Ha et al. (Ha)	5,136,188	Aug. 4, 1992
Agrawal et al. (Agrawal)	5,225,719	Jul. 6, 1993

Claims 1-15, 17-22, and 24-28 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Agrawal.

Claims 16 and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Agrawal in view of Ha.

Rather than reiterate the conflicting viewpoints advanced by the examiner and appellants regarding the above-noted rejections, we make reference to the examiner's answer (Paper No. 15, mailed October 30, 1997) for the examiner's complete reasoning in support of the rejections, and to appellants' brief (Paper No. 14, filed September 8, 1997) and reply brief<sup>2</sup> (Paper No. 16, filed January 5, 1998) for appellants' arguments thereagainst. Only those arguments actually made by appellants have been considered in this decision. Arguments which appellants could have made but chose not to make in the brief have not been considered. See 37 CFR 1.192(a).

#### OPINION

In reaching our decision in this appeal, we have carefully considered the subject matter on appeal, the rejections advanced

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<sup>2</sup> We observe that the language at the end of page 6 does not correlate with the language beginning on page 7 of the reply brief. However, because appellants position is clear, we decline to request clarification under 37 CFR § 1.196(d).

by the examiner, and the evidence of obviousness relied upon by the examiner as support for the rejections. We have, likewise, reviewed and taken into consideration, in reaching our decision, appellants' arguments set forth in the briefs along with the examiner's rationale in support of the rejections and arguments in rebuttal set forth in the examiner's answer.

It is our view, after consideration of the record before us, that the evidence relied upon and the level of skill in the particular art would not have suggested to one of ordinary skill in the art the invention as set forth in claims 1-28.

Accordingly, we reverse.

In rejecting claims under 35 U.S.C. § 103, it is incumbent upon the examiner to establish a factual basis to support the legal conclusion of obviousness. See In re Fine, 837 F.2d 1071, 1073, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). In so doing, the examiner is expected to make the factual determinations set forth in Graham v. John Deere Co., 383 U.S. 1, 17, 148 USPQ 459, 467 (1966), and to provide a reason why one having ordinary skill in the pertinent art would have been led to modify the prior art or to combine prior art references to arrive at the claimed invention. Such reason must stem from some teaching, suggestion or implication in the prior art as a whole or knowledge generally

available to one having ordinary skill in the art. Uniroyal, Inc. v. Rudkin-Wiley Corp., 837 F.2d 1044, 1051, 5 USPQ2d 1434, 1438 (Fed. Cir. 1988); Ashland Oil, Inc. v. Delta Resins & Refractories, Inc., 776 F.2d 281, 293, 227 USPQ 657, 664 (Fed. Cir. 1985); ACS Hosp. Sys., Inc. v. Montefiore Hosp., 732 F.2d 1572, 1577, 221 USPQ 929, 933 (Fed. Cir. 1984). These showings by the examiner are an essential part of complying with the burden of presenting a prima facie case of obviousness. Note In re Oetiker, 977 F.2d 1443, 1445, 24 USPQ2d 1443, 1444 (Fed. Cir. 1992). If that burden is met, the burden then shifts to the applicant to overcome the prima facie case with argument and/or evidence. Obviousness is then determined on the basis of the evidence as a whole. See id.; In re Hedges, 783 F.2d 1038, 1039, 228 USPQ 685, 686 (Fed. Cir. 1986); In re Piasecki, 745 F.2d 1468, 1472, 223 USPQ 785, 788 (Fed. Cir. 1984); and In re Rinehart, 531 F.2d 1048, 1052, 189 USPQ 143, 147 (CCPA 1976).

We consider first the rejection of claims 1-15, 17-22, and 24-28 under 35 U.S.C. § 103(a) based upon the teachings of Agrawal. With respect to independent claim 1, the examiner's position (answer, pages 5 and 6) is that Agrawal does not show the predetermined number of product term clusters accessible to each output line to be at least twenty product terms. The

examiner adds (answer, page 6) that appellants' invention allows routing of more product terms to each output line by using larger demultiplexers and correspondingly larger logic gates than Agrawal. The examiner asserts (id.) that:

Demultiplexers and logic gates are notoriously well-known in the art of digital logic design and can be designed to provide varying numbers of outputs and inputs, respectively, by way of well-known design techniques (i.e., basic CMOS design).

Thus, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to have increased the numbers of the product terms routed to each output line as a matter of design choice in order to increase and/or optimize the programmability of the logic allocator of Agrawal.

In the examiner's view, (id.) the number of routable product terms available to each output is a result effective variable which depends upon the sizing of the demultiplexer and logic circuits, and appellants appear "merely to be optimizing the device to include a particular, optimal value of product[-]terms available to each output." With regard to independent claims 13 and 28, the examiner's position (answer, page 7) is that Agrawal does not disclose each output line having programmable access to at least five input lines. The examiner asserts (id.) that "[s]imilarly as above, it would have been obvious to one of ordinary skill in the art at the time of applicant's invention to

have increased the numbers of its input lines routed to each of the output lines as a matter of design choice to optimize programmability."

Upon careful review of the entire record, we find, for the reasons which follow, that the examiner has failed to establish a prima facie case of obviousness of independent claims 1, 13, and 28; and agree with the position set forth by appellants in the brief and reply brief.

Appellants assert (brief, page 9) that the examiner's proposed modification of the programmability of the logic allocator is a conclusionary, simplistic comment that contradicts the disclosure of Agrawal of providing optimum balance between functionality, silicon die size and performance, and (brief, page 10) Agrawal's teaching that speed performance of the device is important.

The examiner acknowledges (answer, page 10) that the state of the art optimizes according to the variables that appellants have stated, but asserts that "improvements in any one of functionality, silicon die size and performance (i.e. speed) all involve corresponding tradeoffs with regard to the other factors." In the examiner's view (answer, page 11):

[An] ordinarily skilled artisan would be motivated to improve programmability (or functionality) at the expense of some speed performance if the improvement in programmability is critical or important to the application at hand while the corresponding decrease in speed is not as critical or important.

We find that Agrawal discloses (col. 5, lines 19 and 20) that "[f]or a high density PAL-like device[,] achieving higher speed is extremely critical." Agrawal further discloses (col. 5, lines 29-32) that the programmable logic device "gives an optimum balance between functionality, silicon die size, and performance."

From the disclosure of Agrawal that speed is critical and that an optimum balance should be provided between functionality, silicon die size and performance, we find no suggestion to increase functionality (programmability or routability) at the expense of performance (speed) by modification of the logic allocator to provide each output line of the logic allocator with programmable access to the claimed numbers of product-terms and input lines. As noted by appellants (reply brief, page 5):

In the instant invention, Applicants did not optimize programmability at the expense of speed as hypothesized by the Examiner. Rather, "[a] programmable optimized-distribution logic allocator ... enhances the speed, silicon utilization, logic efficiency, logic utilization, and scalability of very high-density complex PLDs that use[s] the new logic allocator."

In addition, we find the examiner's reliance on In re Boesch, 617 F.2d 272, 276, 205 USPQ 215, 219 (CCPA 1980) to be misplaced, as the examiner has not pointed to any disclosure in Agrawal, or within the knowledge of an artisan that would teach or suggest the kind of experimentation necessary to achieve the claimed product terms or input lines for each output line of the logic allocator. As noted by appellants (brief, pages 13 and 14) the benefits of providing the claimed programmability (as disclosed on pages 13 and 14 of appellants' specification) is that:

First, the need for "wrap-around" at the boundaries of the programmable logic array for better product-term allocation has been obviated. Second, the need for an output switch matrix between the logic macrocells and the I/O cells also has been obviated . . . . The programmable optimized-distribution logic allocator achieves the flexibility of optimal routability of logic product-term clusters to I/O pins which allows retaining a prior pin-out while changing a logic design. In addition, the twenty logic product terms can be routed to a particular logic macrocell without any additional speed penalty. This number of product terms is typically sufficient to allow complete shuffling of the logic mapped on the PLD with the ability to retain prior pin-outs and removes any dependencies of product-term clusters between adjacent macrocells.

In addition, the fact that demultiplexers and logic gates are well known in the art of digital logic design does not, by itself, provide a teaching or suggestion of the specific number

of product-terms or input lines available to each output line of the logic allocator recited in appellants' claims. The examiner has not pointed to any showing in Agrawal that would teach or suggest any modification of the logic allocator by changing the demultiplexers and logic gates to provide the logic allocator with programmable access to the claimed numbers of product terms and input lines. From all of the above, we find the examiner's broad, conclusionary statements to be unsupported by evidence in the record. We therefore conclude that the examiner has failed to establish a prima facie case of obviousness of independent claims 1, 13, and 28. Accordingly, the rejection of claims 1, 13, and 28, as well as dependent claims 2-12, 14, 15, 17-22, and 24-27 under 35 U.S.C. § 103(a) is reversed.

We turn next to the rejection of dependent claims 16 and 23 under 35 U.S.C. § 103(a), where the examiner additionally relies upon Ha as evidence of obviousness. We reverse the rejection of claims 16 and 23 under 35 U.S.C. § 103(a) as the examiner has not pointed to any teaching in Ha that would make up for the basic deficiencies of Agrawal.

CONCLUSION

To summarize, the decision of the examiner to reject claims 1-28 under 35 U.S.C. § 103(a) is reversed.

REVERSED

JERRY SMITH	)	
Administrative Patent Judge	)	
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	)	BOARD OF PATENT
ANITA PELLMAN GROSS	)	APPEALS
Administrative Patent Judge	)	AND
	)	INTERFERENCES
	)	
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STUART S. LEVY	)	
Administrative Patent Judge	)	

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