

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

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Paper No. 21

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE BOARD OF PATENT APPEALS  
AND INTERFERENCES

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Ex parte ALEXANDER KALNITSKY

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Appeal No. 1999-0382  
Application 08/436,133<sup>1</sup>

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ON BRIEF

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Before BARRETT, FLEMING, and LEVY, Administrative Patent Judges.  
BARRETT, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the final rejection of claims 1-4 and 6-18. Claim 5 has been canceled.

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<sup>1</sup> Application for patent filed May 8, 1995, entitled "Method of Via Formation for Multilevel Interconnect Integrated Circuits," which is a division of Application 08/329,767, filed October 27, 1994, now U.S. Patent 5,470,793, issued November 28, 1995, which is a continuation of Application 08/036,229, filed March 24, 1993, now abandoned, which is a continuation of Application 07/726,792, filed June 28, 1991, now abandoned.

We reverse.

BACKGROUND

The disclosed invention relates to an interconnect structure for a semiconductor integrated circuit in which the top dielectric layer has voids.

Claim 1 is reproduced below.

1. A contact structure on a semiconductor integrated circuit, comprising:

a conductive element;

a first dielectric layer overlying said conductive element;

a second dielectric layer overlying said first dielectric layer;

a third dielectric layer overlying said second dielectric layer, said third dielectric layer containing voids which allow a chemical wet etch to pass through said third dielectric layer to said second dielectric layer, wherein said second dielectric layer is made of material having a slower etching speed than said third dielectric layer;

an opening through said first, second and third dielectric layers to expose a portion of said conductive element; said opening having an upper portion and a lower portion wherein the upper portion of said opening is the result of a chemical wet etch;

a second conductive element overlying portions of said third dielectric layer and extending into said opening; wherein said second conductive element makes electrical contact with said first conductive element.

The Examiner relies on the admitted prior art (APA) of Appellant's figures 1 and 2 and on the following prior art:

Koyama et al. (Koyama)                      5,200,808                      April 6, 1993

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(effective filing date September 7, 1990)  
Nagamine et al. (Nagamine) 5,319,246 June 7, 1994  
(effective filing date September 7, 1990)

Claims 1-4 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama.

Claims 6 and 7 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Koyama further in view of the APA.

Claims 8-18 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over the APA and Nagamine.

We refer to the final rejection (Paper No. 7) (pages referred to as "FR\_\_") and the examiner's answer (Paper No. 15) (pages referred to as "EA\_\_") for a statement of the Examiner's position, and to the brief (Paper No. 14) (pages referred to as "Br\_\_") and the reply brief (Paper No. 16) (pages referred to as "RBr\_\_") for a statement of Appellant's arguments thereagainst.

#### OPINION

##### Grouping of claims

Appellant groups the claims as follows (Br5):

Group A: claims 1-4, 6, 7, and 16-18 stand or fall together with independent claim 1; and

Group B: claims 8-18 stand or fall together with independent claim 8.

The Examiner disagrees with the grouping "because there is an overlap in the two desired groups" (EA3). In particular, it can be seen that claims 16-18 overlap between groups.

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Appellant argues that the groupings are proper (RBr4), but does not explain how claims 16-18, which depend on claim 8, can be logically grouped to stand or fall together with the rest of the claims of Group A which depend from claim 1. Accordingly, we find that Group A includes only claims 1-4, 6, and 7.

Group A - claims 1-4, 6, and 7

Initially, in the limitation "said third dielectric layer containing voids which allow a chemical wet etch to pass through said third dielectric layer to said second dielectric layer," we interpret "which allow a chemical wet etch to pass through said third dielectric layer to said second dielectric layer" to be like a whereby clause which indicates that voids will necessarily give this result if the area of the third dielectric layer contained voids is subjected to a wet etch. The limitation is met even if voids do not occur at a location, such as the location of a contact via, which is actually etched. No actual chemical wet etch step is recited.

The issue is whether Koyama teaches or suggests "said third dielectric layer containing voids."

The Examiner finds (FR3; EA4): "As stated in the specification, 'voids' occur because of the inherent nature of the material." Appellant does not disagree. However, Appellant argues, voids do not inherently occur in every dielectric or

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silicon oxide layer, but selection of the appropriate materials and processes, known to those skilled in the art, will result in a dielectric layer having voids (Br7). The Examiner acknowledges that voids may not occur in every silicon dioxide layer (EA9).

Based on these arguments, we find that voids are not inherent in every dielectric or silicon oxide layer.

The Examiner states that "[the voids] were not affirmatively incorporated in the material by any method disclosed by the Applicant" (FR3; EA4). The Examiner further states (EA8):

In claim one, there is no mention of a manufacturing process that forms the third dielectric layer - none. Further, there are no processes indicated in claim one that were relied upon to form voids in the dielectric layer. According to the claim, the voids simply exists [sic] in the dielectric layer. The language in claim one simply states, "said third dielectric layer containing voids."

Appellant responds that the Examiner's statements are correct because voids are a structural limitation (RBr5).

The voids are a structural limitation. Claim 1 is an apparatus claim (strictly speaking a product-by-process claim) and it does not need to recite the material or process of producing "said third dielectric layer containing voids."

The Examiner states (EA4): "Therefore, since the material of the prior art is the same as the one claimed, the prior art is also considered to have 'voids'." The Examiner acknowledges that voids may not occur in every silicon dioxide layer, but states that the specification discloses deposition of an oxide at

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page 6, lines 28-31, which supports the conclusion that depositing the same material as the one specified in the specification would (inherently) lead to voids (EA9).

Koyama discloses that "the overlying film 20 (silicon oxide film) is formed on the overall surface of the intermediate film 19" (emphasis added) (col. 7, lines 53-55). Appellant discloses that the third dielectric layer material is "preferably an undoped CVD oxide layer" (specification, p. 7, lines 23-24) and this is the only material specified. Appellant argues that Koyama does not disclose use of the same process disclosed by Appellant (Br7-8), i.e., the CVD process. Appellant further argues that Koyama only states that the overlying oxide film is "formed" and "[n]one of the references of record indicate that the silicon oxide layers corresponding to the claimed third dielectric layer are formed by deposition" (RBr6).

We think the disclosure in Koyama that the silicon oxide layer is "formed" implies that the layer is "deposited." How else can the silicon oxide be formed? Because the silicon oxide is formed on a silicon nitride layer, the silicon oxide is not going to be grown as a thermal oxide. Nevertheless, there is insufficient evidence to establish that the silicon oxide layer in Koyama inherently has voids because we do not know that all methods of "forming" will produce voids. The Examiner's finding that Koyama's silicon oxide layer inherently would have voids is

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unsupported speculation. See In re Warner, 379 F.2d 1011, 1017, 154 USPQ 173, 178 (CCPA 1967) (it is improper to resort to speculation or unfounded assumptions to supply deficiencies in the factual basis for a rejection). We conclude that the Examiner has failed to establish a prima facie case of obviousness as to the limitation of "said third dielectric layer containing voids." Accordingly, the rejection of claims 1-4, 6, and 7 is reversed.

Group B - claims 8-18

The Examiner finds that the APA teaches the claimed invention except for a second conductive layer and a fourth dielectric layer (FR6; EA7). The Examiner finds that Nagamine discloses the use of second conductive layer and concludes that it would have been obvious to provide a second electrically conductive layer to facilitate electrical communication within the semiconductor device (FR6; EA7). The Examiner finds that Nagamine teaches the use of a conformal silicon nitride layer sandwiched between two oxide layers and concludes that "it would have been obvious to one of ordinary skill in the art to provide the Appellant's disclosed prior art with a silicon nitride layer of oxide to preserve the structural integrity of the contact structure" (FR6; EA7).

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The second conductive layer is not argued. In any case, APA figure 2 implies the existence of a second conductive layer.

Appellant argues that Nagamine does not provide any motive or incentive to make the proposed modification of adding a fourth dielectric layer (Br9-10). The Examiner responds that the motivation need not be expressly stated in the references and that Nagamine discloses a conformal silicon nitride layer sandwiched between two oxide layers (EA11).

While we agree with the Examiner that the motivation need not be expressly stated in the reference, there needs to be some good reason in the reference or in the knowledge of one of ordinary skill in the art why one skilled in the art would have sought to make the proposed modification. Nagamine discloses (col. 2, lines 38-40): "The intermediate film 19 is an extension of a capacitor dielectric film, for example, a silicon nitride film." See also col. 7, lines 13-15. Because the purpose of the silicon nitride layer in Nagamine is not to act as an etch stop layer to prevent damage to the contact, we fail to find any motivation for the Examiner's conclusion that "it would have been obvious to one of ordinary skill in the art to provide the Appellant's disclosed prior art with a silicon nitride layer of oxide to preserve the structural integrity of the contact structure" (FR6; EA7). It is noted that unlike the corresponding "second dielectric layer" claim 1, which is claimed to be "made

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of material having a slower etch speed than said third dielectric layer," the "fourth dielectric layer" of claim 8 does not have a comparable limitation: the layer could be any dielectric material. We conclude that the Examiner has failed to show motivation for the addition of a silicon nitride layer in the APA and has failed to establish a prima facie case of obviousness. Accordingly, the rejection of claims 8-18 is reversed.

CONCLUSION

The rejections of claims 1-4 and 6-18 are reversed.

REVERSED

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|-----------------------------|---|-----------------|
| LEE E. BARRETT              | ) |                 |
| Administrative Patent Judge | ) |                 |
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|                             | ) | BOARD OF PATENT |
| MICHAEL R. FLEMING          | ) | APPEALS         |
| Administrative Patent Judge | ) | AND             |
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| STUART S. LEVY              | ) |                 |
| Administrative Patent Judge | ) |                 |

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