

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 19

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte HACK-BIN KIM

Appeal No. 1999-1116
Application No. 08/635,170

HEARD: November 7, 2001

Before KRASS, DIXON, and BLANKENSHIP, Administrative Patent Judges.

BLANKENSHIP, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal under 35 U.S.C. § 134 from the examiner's final rejection of claims 1-14, which are all the claims in the application.

We reverse.

BACKGROUND

The invention is directed to a process for preventing sequencer overrun, which is an error condition in a disk controller. Claim 1 is reproduced below.

1. A sequencer overrun prevention method, comprising the steps of:
initializing a sequencer;
reading a timer value indicating when said sequencer begins operation;
calculating a sequencer halting point by adding a predetermined time constant to said timer value;
determining whether said sequencer operates at said sequencer halting point; and
forcibly halting said sequencer when said sequencer operates at said sequencer halting point.

The examiner relies on the following reference:

Machado et al. (Machado)	5,517,631	May 14, 1996 (filed Jul. 7, 1993)
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Claims 1-14 stand rejected under 35 U.S.C. § 102 as being anticipated by Machado.

We refer to the Final Rejection (mailed Dec. 12, 1997) and the Examiner's Answer (mailed Sep. 1, 1998) for a statement of the examiner's position and to the Brief (filed June 15, 1998) and the Reply Brief (filed Oct. 29, 1998) for appellant's position with respect to the claims which stand rejected.

OPINION

The examiner's statement of the rejection of instant claim 1 as being anticipated by Machado is set forth on page 3 of the Answer. Appellant agrees with the majority of the examiner's findings with respect to the disclosure of Machado (Brief at 4-5). Appellant contends, however, that there is no disclosure of using a timer value, calculating a sequencer halting point, and halting the sequencer when the sequencer operates at the sequencer halting point, as required by claim 1.

In the initial statement of the rejection (Answer at 3), Machado's loop counter 240 (Fig. 6B) is deemed to correspond to "calculating a sequencer halting point by adding a predetermined time constant...to the timer value." In the response to appellant's arguments, however, the examiner (id. at 5) refers to index timeout counter 242 (Fig. 6B) as generating an index timeout value, and refers to column 17, lines 50 through 67 of the reference. In the Reply Brief (at 2-3), appellant disagrees with any suggestion that the index timeout counter 242 corresponds to the claimed calculation of adding a predetermined time constant to the timer value.

Machado discloses a sequencer 152 (Fig. 5) as an element of circuit 140. Figures 6A and 6B show details of sequencer 152. The loop counter 240 is preset with the number of loops to be made during a particular block transfer transaction, and generates a

LOOPCNT=0 control value when the count reaches zero. Machado at col. 17, ll. 50-54.

Loop counter 240 is decremented by signal ISDL. See id. at Fig. 6B and col. 26. ll. 61-62.

Index timeout counter 242 (Fig. 6B) is a counter similar to loop counter 240. A once-per-revolution index signal is used to clock the index timeout counter, and timeout counter 242 generates an index timeout value, "INXTCNT=0." Id. at col. 17, ll. 57-63. According to column 19, lines 25 through 29 of the reference, the index timeout count specifies the maximum number of index pulses that may occur while sequencer 152 is trying to complete its program.

Neither the loop counter nor the index timeout counter, however, add "a predetermined time constant to [the] timer value," as recited in instant claim 1. The examiner refers (Answer at 3) to column 13, line 48 of the reference as disclosing the reading of a timer value. Machado at column 13, lines 40 through 62 describes the servo data decoder circuit 142 (Fig. 5; an element of circuit 140) as including a "sector timer" which puts out expected servo sector times within circuit 140 based upon detection of each servo address mark. While the section might suggest that circuit 140 utilizes a "timer value" and a "predetermined time constant" in a determination with respect to halting the sequencer to prevent overrun, Machado does not expressly disclose that which is required by instant claim 1.

The examiner contends (Answer at 5) that the "forcible halting" of the sequencer "must involve timing, as a sequencer interrupt is only forced if enabled. The 'enable' latch

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corresponds to the timeout limit." However, as appellant points out on page 2 of the Reply Brief, it is unclear to what "latch" the examiner refers. Moreover, we agree with appellant that there is no clear disclosure of steps in the operation that results in the setting of bit 0 (Machado col. 21, ll. 1-7), forcing the sequencer to halt. Considering the teachings of Machado as a whole, it appears more likely that the sequencer is halted as a result of the counting of block transfers and index signals, rather than as a result of a timer value method as set forth in claim 1.

Anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim. Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co., 730 F.2d 1452, 1458, 221 USPQ 481, 485 (Fed. Cir. 1984). Since the Machado reference does not expressly disclose the method of instant claim 1, and there has been no showing that the apparatus necessarily must perform the steps required by the claim, we cannot sustain the section 102 rejection of claim 1, nor that of the claims depending therefrom.

Each of instant claims 3 and 9 requires "forcibly halting said sequencer when said sequencer halting point is equal to said incremented timer value." The rejection (Answer at 3-4) suffers from a similar deficiency as that applied against claim 1. While there may be a "timer value" associated with servo data decoder circuit 142 (Machado col. 13), the rejection fails to show how the timer value may be incremented and used in determining the halting of the sequencer. The counters shown in Machado's Figure 6B (e.g., sequence

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counter 236), upon which the rejection relies, are not disclosed as comparing an "incremented timer value," but are disclosed as sending signals upon counting the number of loops to be made during a particular data block transfer transaction, upon counting index signals, and upon counting byte sequences. Machado at col. 17, ll. 50-67.

We therefore cannot sustain the section 102 rejection of independent claims 3 and 9, and thus cannot sustain the rejection of any of claims 1-14. Although Machado discloses (column 13) a sector timer, and suggests that other timing functions are performed (e.g., column 29, lines 1-9), we agree with appellant that not each and every element, as arranged in the claims, has been shown to be expressly or inherently disclosed by the reference.

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CONCLUSION

The rejection of claims 1-14 under 35 U.S.C. § 102 is reversed.

REVERSED

ERROL A. KRASS)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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)	
)	
HOWARD B. BLANKENSHIP)	
Administrative Patent Judge)	

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Robert E. Bushnell
Suite 300
1522 K ST NW
Washington, DC 20005-1202