

The opinion in support of the decision being entered today was not written for publication and is not binding precedent of the Board.

Paper No. 10

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JOHN HUDAK and THOMAS R. NEAL

Appeal No. 1999-2571
Application No. 08/820,200

HEARD: October 11, 2001

Before BARRETT, DIXON, and GROSS, Administrative Patent Judges.
GROSS, Administrative Patent Judge.

DECISION ON APPEAL

This is a decision on appeal from the examiner's final rejection of claims 1, 3, 5 through 11, and 13 through 19, which are all of the claims pending in this application.

Appellants' invention relates to a method of making a semiconductor device using an SOI starting wafer and thinning process with a non-SOI semiconductor fabrication process selected from CMOS, NMOS, PMOS, Bipolar, and BICMOS fabrication processes. Claim 1 is illustrative of the claimed invention, and it reads as follows:

Appeal No. 1999-2571
Application No. 08/820,200

1. A method of making a semiconductor device using an SOI starting wafer and thinning the same, comprising the steps of:

a) receiving the SOI starting wafer, where the SOI starting wafer includes a silicon substrate and an oxide layer thereon;

b) selecting a semiconductor fabrication process for fabricating the semiconductor device from a group of semiconductor fabrication processes consisting of CMOS, NMOS, PMOS, Bipolar, and BICMOS;

c) forming a layer of device quality silicon on the oxide layer of the SOI starting wafer to a sufficient thickness and doping profile to realize the semiconductor device;

d) fabricating the semiconductor device in the device quality silicon layer using the semiconductor fabrication process selected;

e) forming a support layer on the device quality silicon layer having the semiconductor device fabricated therein; and

f) thinning the result of step (e).

The prior art references of record relied upon by the examiner in rejecting the appealed claims are:

Sharma et al. (Sharma) 1994	5,344,524	Sep. 06,
McCarthy 1997	5,674,758	Oct. 07,

(filed Jun. 06, 1995)

Appeal No. 1999-2571
Application No. 08/820,200

Claims 1, 3, 5 through 11, and 13 through 19 stand rejected under 35 U.S.C. § 103 as being unpatentable over Sharma in view of McCarthy.¹

Reference is made to the Examiner's Answer (Paper No. 6, mailed April 6, 1999) for the examiner's complete reasoning in support of the rejections, and to appellants' Brief (Paper No. 5, filed February 23, 1999) for appellants' arguments thereagainst.

OPINION

We have carefully considered the claims, the applied prior art references, and the respective positions articulated by appellants and the examiner. As a consequence of our review, we will reverse the obviousness rejection of claims 1, 3, 5 through 11, and 13 through 19.

Independent claims 1 and 19 recite the steps of "selecting a semiconductor fabrication process for fabricating the semiconductor device from a group of semiconductor fabrication processes consisting of CMOS, NMOS, PMOS, Bipolar,

¹ The examiner (Answer, page 3) withdraws the rejection of claims 1, 3, 5 through 11, and 13 through 19 under 35 U.S.C. § 112, second paragraph. Also, the examiner omits in the Answer the rejection of claims 1, 3, 5 through 11, and 13 through 19 under 35 U.S.C. § 103 over Sharma, McCarthy, and Sze. Thus, only the rejection of claims 1, 3, 5 through 11, and 13 through 19 under 35 U.S.C. § 103 over Sharma and McCarthy remains before us on appeal.

Appeal No. 1999-2571
Application No. 08/820,200

and BICMOS" and using the selected process to form the semiconductor device. The recited processes are non-SOI fabrication processes, as explained in appellants' specification (page 3, lines 2-4). CMOS, NMOS, PMOS, Bipolar, and BICMOS circuits may be formed by such non-SOI processes or by SOI processes such as silicon-on-sapphire. Thus, disclosure of a CMOS, NMOS, PMOS, Bipolar, or BICMOS circuit does not equate to a disclosure of a CMOS, NMOS, PMOS, Bipolar, or BICMOS fabrication process.

Turning to the rejection, we find that the examiner (Answer, page 3) relies on Sharma (column 1, lines 53-58, and column 4, lines 30-34) as a teaching to select and use a CMOS or Bipolar semiconductor device fabrication process. However, Sharma states (column 1, lines 5-8) that the invention "pertains to silicon-on-insulator (SOI) transistor technology." Sharma (column 1, lines 9-58) goes on to discuss SOI fabrication processes and the resulting CMOS and Bipolar circuits. Thus, Sharma relates to CMOS and Bipolar circuits formed by SOI fabrication processes, not by CMOS and Bipolar (non-SOI) processes.

Appeal No. 1999-2571
Application No. 08/820,200

In column 4, lines 30-34, Sharma states that the wafer is processed "through the conventional CMOS/Bipolar process sequence using conventional SOI device processing technologies." Although we appreciate how the examiner read the language used in this excerpt as suggesting CMOS or Bipolar fabrication processes, as the language is ambiguous, it is clear in light of the portion discussed above that Sharma means that CMOS/Bipolar circuits are formed using SOI processes. Accordingly, Sharma fails to disclose the steps of choosing and using one of the recited non-SOI fabrication processes to form a semiconductor device. As McCarthy does not cure this deficiency, no *prima facie* case of obviousness has been established, and we cannot sustain the rejection of claims 1 and 19 nor of their dependents, claims 3, 5 through 11, and 13 through 18.

Appeal No. 1999-2571
Application No. 08/820,200

CONCLUSION

The decision of the examiner rejecting claims 1, 3, 5 through 11, and 13 through 19 under 35 U.S.C. § 103 is reversed.

REVERSED

LEE E. BARRETT)	
Administrative Patent Judge)	
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)	BOARD OF PATENT
JOSEPH L. DIXON)	APPEALS
Administrative Patent Judge)	AND
)	INTERFERENCES
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ANITA PELLMAN GROSS)	
Administrative Patent Judge)	

apg/vsh

Appeal No. 1999-2571
Application No. 08/820,200

PATENT COUNSEL
NATIONAL SECURITY AGENCY
9800 SAUAGE ROAD SUITE 6542
FT MEADE, MD 20755-6542