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| To: | Mail Stop 8<br>Director of the U.S. Patent and Trademark Office<br>P.O. Box 1450<br>Alexandria, VA 22313-1450 | <b>REPORT ON THE<br/>                 FILING OR DETERMINATION OF AN<br/>                 ACTION REGARDING A PATENT OR<br/>                 TRADEMARK</b> |
|-----|---|--|

In Compliance with 35 U.S.C. § 290 and/or 15 U.S.C. § 1116 you are hereby advised that a court action has been filed in the U.S. District Court United States District Court for the Western District of Washington on the following:  Patents or  Trademarks:

| DOCKET NO.                              | DATE FILED              | US District Court United States District Court for the Western District of Washington |
|---|-------------------------|---|
| 2:08-cv-01373-MJP                       | 9/12/08                 |   |
| PLAINTIFF                               |                         | DEFENDANT   |
| Wistron Corporation                     |                         | Samsung Electronics Co Ltd<br>et al.  |
| PATENT OR TRADEMARK NO.                 | PATENT OR TRADEMARK NO. | PATENT OR TRADEMARK NO.   |
| 1. See attached page for patent numbers | 6.                      | 11.   |
| 2.                                      | 7.                      | 12.   |
| 3.                                      | 8.                      | 13.   |
| 4.                                      | 9.                      | 14.   |
| 5.                                      | 10.                     | 15.   |

In the above-entitled case, the following patents(s)/ trademark(s) have been included:

| DATE INCLUDED           | INCLUDED BY  |                         |
|-------------------------|--|-------------------------|
|                         | Amendment <input type="checkbox"/> Answer <input type="checkbox"/> Cross Bill <input type="checkbox"/> Other Pleading <input type="checkbox"/> |                         |
| PATENT OR TRADEMARK NO. | PATENT OR TRADEMARK NO.  | PATENT OR TRADEMARK NO. |
| 1.                      | 6.   | 11.                     |
| 2.                      | 7.   | 12.                     |
| 3.                      | 8.   | 13.                     |
| 4.                      | 9.   | 14.                     |
| 5.                      | 10.  | 15.                     |

In the above-entitled case, the following decision has been rendered or judgment issued:

|                   |
|-------------------|
| DECISION/JUDGMENT |
|-------------------|

|              |                   |         |
|--------------|-------------------|---------|
| CLERK        | (BY) DEPUTY CLERK | DATE    |
| Bruce Rifkin | MKB               | 9/16/08 |



08-CV-01373-CMP

FILED ENTERED  
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SEP 12 2008

AT SEATTLE  
CLERK U.S. DISTRICT COURT  
WESTERN DISTRICT OF WASHINGTON  
DEPUTY

UNITED STATES DISTRICT COURT  
WESTERN DISTRICT OF WASHINGTON  
AT SEATTLE

WISTRON CORPORATION, a Taiwan  
corporation,

Plaintiff,

v.

SAMSUNG ELECTRONICS CO., LTD., a  
Republic of Korea corporation; SAMSUNG  
ELECTRONICS AMERICA, INC., a New York  
corporation; and SAMSUNG  
TELECOMMUNICATIONS AMERICA, LLC,  
a Delaware limited liability company;

Defendants.

Case No.

**C 08-1373** MJP

**COMPLAINT FOR INFRINGEMENT  
U.S. PATENT NOS. 5,410,713;  
5,870,613; AND 5,903,765**

**JURY TRIAL DEMANDED**

*Summ. Iss. SEA 20477*

Plaintiff WISTRON CORPORATION ("Wistron") complains of Defendants  
SAMSUNG ELECTRONICS CO., LTD. ("SEC"), SAMSUNG ELECTRONICS AMERICA,  
INC. ("SEA"), and SAMSUNG TELECOMMUNICATIONS AMERICA, LLC ("STA")  
(collectively, "Defendants") and by this Complaint alleges as follows.

**PARTIES**

1. Wistron is a corporation organized in 2001, and existing under the laws of  
Taiwan, with its principle place of business in Hsichih, Taiwan. Wistron is an Original  
Design Manufacturing ("ODM") company that designs, develops and manufactures electronic

COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 1

Case No.

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1 products for customers to sell under their own brand name including companies such as  
2 Microsofi, Hewlett Packard, Dell and Lenovo. As a result, Wistron is a leading manufacturer  
3 of personal computers including stand alone PCs, laptops, notebooks and other computing  
4 devices, including computing devices that are sold throughout the United States, including  
5 this district.

6 2. SEC is a corporation organized and existing under the laws of the Republic of  
7 Korea, with its principle place of business at 250 2-ga Taepyong-ro, Jung-gu, Seoul, 100-742,  
8 South Korea. SEC is a member of the multinational conglomerate Samsung Group, which  
9 manufactures and sells electronic products including cell phones, video playback equipment  
10 such as VCRs and DVD players, set top boxes and computers. In 2007, SEC boasted sales  
11 revenues of nearly \$100 billion, with a net income in excess of \$7.4 billion.

12 3. SEA is a New York corporation with its principal place of business at 105  
13 Challenger Park Road, Ridgefield Park, New Jersey 07660. On information and belief, SEA  
14 was formed in 1977 as a subsidiary of SEC, and markets, sells, or offers for sale a variety of  
15 consumer electronics products including video playback equipment, TVs, set top boxes and  
16 all manner of computer components and peripherals. On information and belief, SEA  
17 manages the operations of STA.

18 4. STA is a Delaware limited liability company with its principal place of  
19 business at 1301 East Lookout Drive, Richardson, Texas 75091. On information and belief,  
20 STA was founded in 1996 as a subsidiary of SEC, and markets, sells, or offers for sale a  
21 variety of personal and business communications devices in the United States, including cell  
22 phones.

### 23 JURISDICTION

24 5. This is an action for patent infringement, over which this Court has subject  
25 matter jurisdiction pursuant to 28 U.S.C. §§ 1331 and 1338(a).

26  
COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 2

Case No.

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1 power management systems and methods for computers. A true and correct  
2 copy of the '713 patent is attached hereto as Exhibit 1.

3 b. U.S. Patent No. 5,870,613 entitled "Power Management System for a  
4 Computer," was duly and legally issued on February 9, 1999, from patent  
5 application Serial No. 08/422,599 filed on April 14, 1995, which application  
6 was a continuation of application Serial No. 07/816,108 filed on January 2,  
7 1992 (and that lead to the issuance of the '713 patent), with Dave White, Yen  
8 Wei Lee, Rod Ang, Ray Barbieri, James Chen and Suh Chiueh Lee as the  
9 named inventors (the "'613 patent"). Among other things, the '613 patent  
10 discloses power management systems and methods for computers. A true and  
11 correct copy of the '613 patent is attached hereto as Exhibit 2.

12 c. U.S. Patent No. 5,903,765 entitled "Power Management System for a  
13 Computer," was duly and legally issued on May 11, 1999, from patent  
14 application Serial No. 08/825,663 filed on April 3, 1997, which application  
15 was a division of application No. 08/422,599 (that lead to the issuance of the  
16 '613 patent), which is a continuation of application Serial No. 07/816,108 filed  
17 on January 2, 1992 (that lead to issuance of the '713 patent), with Dave White,  
18 Yen Wei Lee, Rod Ang, Ray Barbieri, James Chen and Suh Chiueh Lee as the  
19 named inventors (the "'765 patent"). Among other things, the '765 patent  
20 discloses power management systems and methods for computers. A true and  
21 correct copy of the '765 patent is attached hereto as Exhibit 3.

22 9. Each of the Wistron Patents is valid and enforceable.

23 10. No later than June 28, 2007, representatives of SEC were put on express  
24 written and oral notice of Wistron's claim that one or more of the Defendants are infringing  
25 the '613 patent. The notice provided by Wistron to SEC included, but was not limited to  
26

COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 4

Case No.

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1 claim charts covering the Samsung Blackjack SGH-i607 and SGH-D307 cell phones. On  
2 information and belief, Defendants have been on notice of the balance of the Wistron Patents  
3 since approximately that time.

4 11. Each of the Defendants has directly and indirectly infringed and continues to  
5 infringe, literally or under the doctrine of equivalents, one or more claims of the Wistron  
6 Patents by acting without authority so as to:

7 a. make, have made, use, offer to sell, sell within the United States, or import into  
8 the United States computer and digital products, that embody or practice the  
9 patented inventions, or practice the patented processes in the United States in  
10 connection with these activities, including at least:

11 i. Samsung SGH-D900 and SGH-D500 cell phones along with any other  
12 cell phones that embody or use the same or equivalent power  
13 management units and/or start up routine technology systems or  
14 methods;

15 ii. Samsung DVD-E217, E218, E219, E317, E319, E135, E535, P213,  
16 P313, E2323 players and any other DVD players that embody or use  
17 the same or equivalent power management units and/or start up routine  
18 technology systems or methods; and

19 iii. Samsung Blu-Ray players, televisions, home theater systems, data  
20 projectors, laser printers, multi-function printers, MP3 players and  
21 UMPC's that embody or use the same or equivalent power  
22 management units and/or start up routine technology systems or  
23 methods as the specific cell phones and DVD players identified above.

24 b. contribute to or actively induce infringement of the Wistron Patents.

25 12. The foregoing products shall be referred to as the Wistron Accused Products  
26

COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 5

Case No.

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1 13. The above-described acts of infringement committed by Defendants have  
2 caused injury and damage to Wistron, and will continue to cause additional severe and  
3 irreparable injury and damages unless Defendants are enjoined from further infringing all of  
4 the foregoing Wistron Patents.

5  
6 **FIRST CLAIM FOR RELIEF**

7 **Infringement of U.S. Patent No. 5,410,713**

8 14. Wistron alleges, and incorporates by reference, the allegations of paragraphs 1  
9 through 13 above.

10 15. Defendants have directly, indirectly, contributorily, and/or by inducement  
11 infringed one or more claims of the '713 patent, literally, and/or under the doctrine of  
12 equivalents as proscribed by 35 U.S.C. § 271. The accused products include the Wistron  
13 Accused Products identified above.

14 16. As a consequence of Defendants' infringement, Wistron is entitled to recover  
15 damages adequate to compensate it for the injuries complained of herein, but in no event less  
16 than a reasonable royalty. Wistron is further entitled to have Defendants enjoined from  
17 committing additional future acts of infringement that would subject Wistron to irreparable  
18 harm.

19 **SECOND CLAIM FOR RELIEF**

20 **Infringement of U.S. Patent No. 5,870,613**

21 17. Wistron alleges, and incorporates by reference, the allegations of paragraphs 1  
22 through 16 above.

23 18. Defendants have directly, indirectly, contributorily, and/or by inducement  
24 infringed one or more claims of the '613 patent, literally, and/or under the doctrine of  
25

26  
COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 6

Case No.

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1 equivalents as proscribed by 35 U.S.C. § 271. The accused products include the Wistron  
2 Accused Products identified above.

3 19. As a consequence of Defendants' infringement, Wistron is entitled to recover  
4 damages adequate to compensate it for the injuries complained of herein, but in no event less  
5 than a reasonable royalty. Wistron is further entitled to have Defendants enjoined from  
6 committing additional future acts of infringement that would subject Wistron to irreparable  
7 harm.

8 **THIRD CLAIM FOR RELIEF**

9 **Infringement of U.S. Patent No. 5,903,765**

10 20. Wistron alleges, and incorporates by reference, the allegations of paragraphs 1  
11 through 19, above.

12 21. Defendants have directly, indirectly, contributorily, and/or by inducement  
13 infringed one or more claims of the '765 patent, literally, and/or under the doctrine of  
14 equivalents as proscribed by 35 U.S.C. § 271. The accused products include the Wistron  
15 Accused Products identified above.

16 22. As a consequence of Defendants' infringement, Wistron is entitled to recover  
17 damages adequate to compensate it for the injuries complained of herein, but in no event less  
18 than a reasonable royalty. Wistron is further entitled to have Defendants enjoined from  
19 committing additional future acts of infringement that would subject Wistron to irreparable  
20 harm.

21 **FOURTH CLAIM FOR RELIEF**

22 **Willful Infringement**

23 23. Wistron alleges and incorporates by reference, the allegations of paragraphs 1  
24 through 22 above.

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COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 7

Case No.

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1 24. As set forth above, since no later than June 28, 2007, representatives of SEC  
2 were notified of several of Wistron's infringement claims under the '613 patent.

3 25. On the face of the '613 patent is a reference to the fact that the underlying  
4 application for said patent was a continuation of the January 2, 1992 application that  
5 ultimately issued as the '713 patent. See Exhibit 2.

6 26. Defendants' representatives should have conducted an analysis of the '613 and  
7 '713 patents in response to having been put on notice of the '613 patent, and therefore did  
8 discover or should have discovered the existence of the '765 patent.

9 27. Defendants' failure to obtain a license to the Wistron Patents and/or failure to  
10 cease their infringing activities was objectively reckless and constitutes willful infringement  
11 of the Wistron Patents for purposes of 35 U.S.C. §§ 284 and 285.

12 **PRAYER FOR RELIEF**

13 WHEREFORE, Wistron prays for relief as follows:

14 1. Entry of a judgment declaring that each of the Defendants has infringed one or  
15 more claims of the Wistron Patents;

16 2. Entry of a preliminary and permanent injunction, pursuant to 35 U.S.C. § 283,  
17 enjoining each of the Defendants, and their respective agents, servants, officers, directors,  
18 employees and all other persons acting in concert with them, directly and indirectly, from any  
19 further acts of infringement, contributory infringement, or inducement of infringement of the  
20 Wistron Patents;

21 3. Entry of a judgment pursuant to 35 U.S.C. § 284 awarding to Wistron damages  
22 to compensate for Defendants' infringements in an amount to be determined at trial (and, if  
23 necessary, related accountings), but not less than a reasonable royalty;

24 4. Entry of a judgment pursuant to 35 U.S.C. § 284 trebling the damages awarded  
25 to Wistron to the extent one or more of the Defendants' infringement has been willful;

26  
COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 8

Case No.

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1           5.     Entry of a judgment pursuant to 35 U.S.C. § 285 declaring that this is an  
2 exceptional case, and awarding Wistron its costs of suit, including reasonable attorney's fees;

3           6.     Entry of a judgment awarding Wistron pre-and post-judgment interest in  
4 accordance with the rates allowed by law; and

5           7.     Any such other and further relief as the Court deems just and proper.  
6

7  
8           DATED: September 12, 2008.

9           By   
10           Douglas B. Greenswag, WSBA # 37506  
11           Martha Rodriguez-Lopez, WSBA # 35466  
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25           Attorneys for Plaintiff  
26           Wistron Corporation

COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 9

Case No.  
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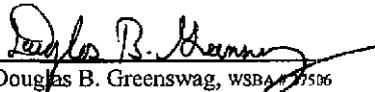
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**JURY TRIAL DEMANDED**

Wistron requests a trial by jury on each cause of action for which a trial by jury is proper.

DATED: September 12, 2008.

By   
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Attorneys for Plaintiff  
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COMPLAINT FOR INFRINGEMENT OF U.S. PATENT  
NOS. 5,410,713; 5,870,613; AND 5,903,765 - 10

Case No.  
K3115644100012020950\_MRL12095072034

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# **EXHIBIT 1**

US005410713A

**United States Patent** [19]

[11] **Patent Number:** **5,410,713**

**White et al.**

[45] **Date of Patent:** **Apr. 25, 1995**

- [54] **POWER-MANAGEMENT SYSTEM FOR A COMPUTER**
- [75] **Inventors:** Dave White; Yen W. Lee; Rod Aug, all of San Jose, Calif.; Ray Barbieri, Campbell, Calif.; James Chen, Taipei, Taiwan, Prov. of China; Suh C. Lee, Palo Alto, Calif.
- [73] **Assignee:** Smith Corona/Acer, New Canaan, Conn.
- [21] **Appl. No.:** 816,108
- [22] **Filed:** Jan. 2, 1992
- [51] **Int. Cl.:** G06F 11/30; H02J 9/00
- [52] **U.S. Cl.:** 395/750; 395/575; 395/725; 364/707; 307/66; 365/226; 365/229
- [58] **Field of Search:** 395/750, 575, 725; 365/226, 229; 364/707; 307/66

|           |        |               |         |
|-----------|--------|---------------|---------|
| 5,220,671 | 6/1993 | Yamagishi     | 395/750 |
| 5,230,074 | 7/1993 | Canova et al. | 395/750 |
| 5,237,692 | 8/1993 | Rasoch et al. | 395/750 |

*Primary Examiner*—Allen R. MacDonald  
*Assistant Examiner*—George Davis  
*Attorney, Agent, or Firm*—Townsend and Townsend Hourie and Crew

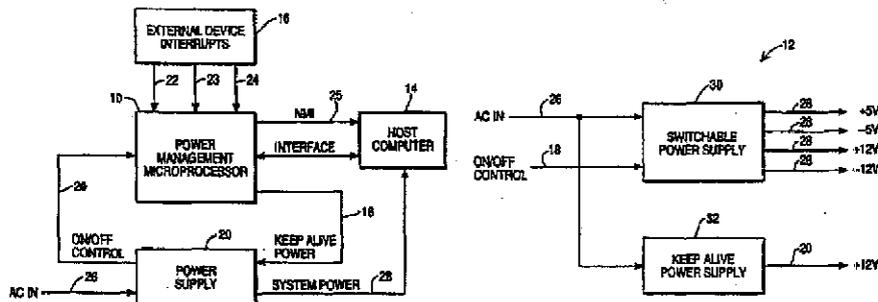
**[57] ABSTRACT**

A power management system for a personal computer comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is powered by the keep alive power supply that continuously provides power. The computer is powered by a power supply that is switchable in response to a control signal. The processor preferably controls the switchable power supply. The processor is coupled to receive external device interrupts from a plurality of external devices that instruct the processor when to turn the switchable power supply on and off. The processor is also coupled to the computer through an interface. The power management system also includes a method for turning the computer on and off. A preferred method uses the processor to control the power provided to the computer. The preferred method also uses the processor to dictate whether the computer will to perform a long boot that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot that brings the computer to an operational state in a much shorter time. A preferred method for turning the computer off includes the ability to exit a program being run by the computer, and saving a hardware state of the computer on a hard disk.

**[56] References Cited**  
**U.S. PATENT DOCUMENTS**

|           |         |                   |         |
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| 4,189,717 | 2/1980  | Takeuchi          | 364/707 |
| 4,200,916 | 4/1980  | Seipp             | 364/900 |
| 4,232,377 | 11/1980 | Tallman           | 365/229 |
| 4,495,569 | 1/1985  | Higawa            | 395/725 |
| 4,551,841 | 11/1985 | Fujita et al.     | 395/750 |
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| 4,611,289 | 9/1986  | Coppola           | 395/750 |
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| 4,675,538 | 6/1987  | Epslein           | 307/66  |
| 4,777,626 | 10/1988 | Matsushita et al. | 365/229 |
| 4,809,163 | 2/1989  | Hirasawa et al.   | 395/750 |
| 4,922,450 | 5/1990  | Rose et al.       | 395/750 |
| 5,121,500 | 6/1992  | Arlington et al.  | 395/750 |
| 5,163,153 | 11/1992 | Cole et al.       | 395/750 |
| 5,167,024 | 11/1992 | Smith et al.      | 395/750 |
| 5,182,810 | 1/1993  | Bartling et al.   | 395/750 |

10 Claims, 5 Drawing Sheets



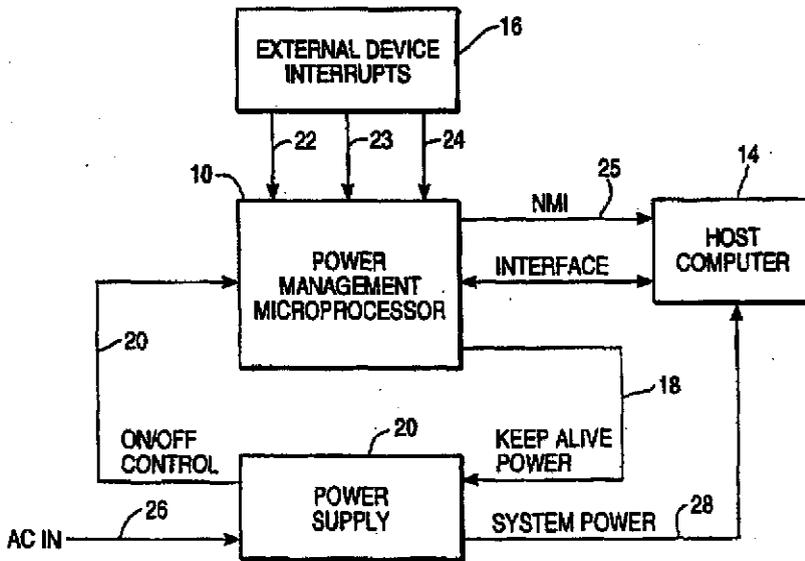


FIG. 1

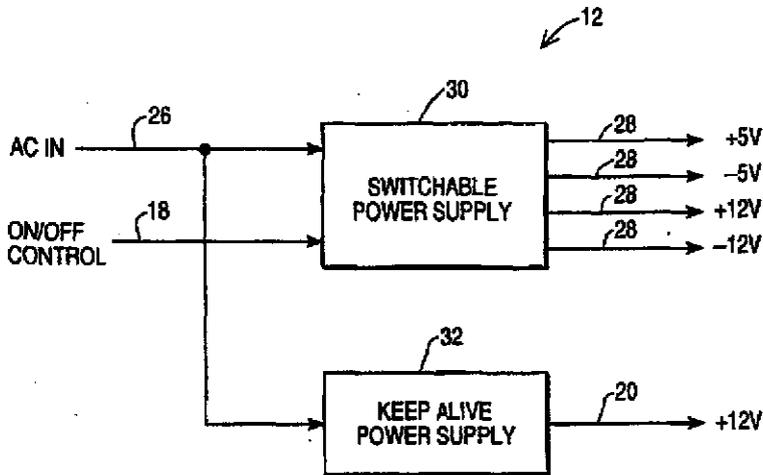


FIG. 2

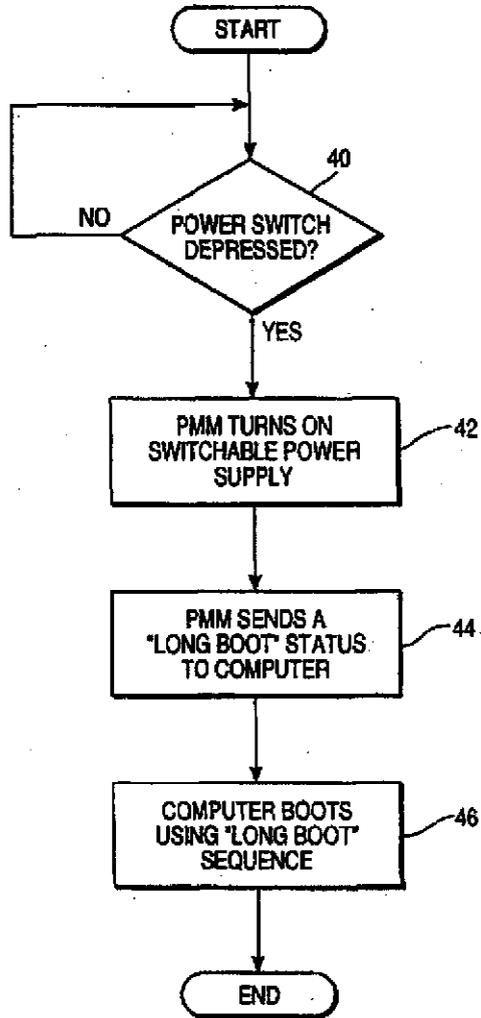


FIG. 3

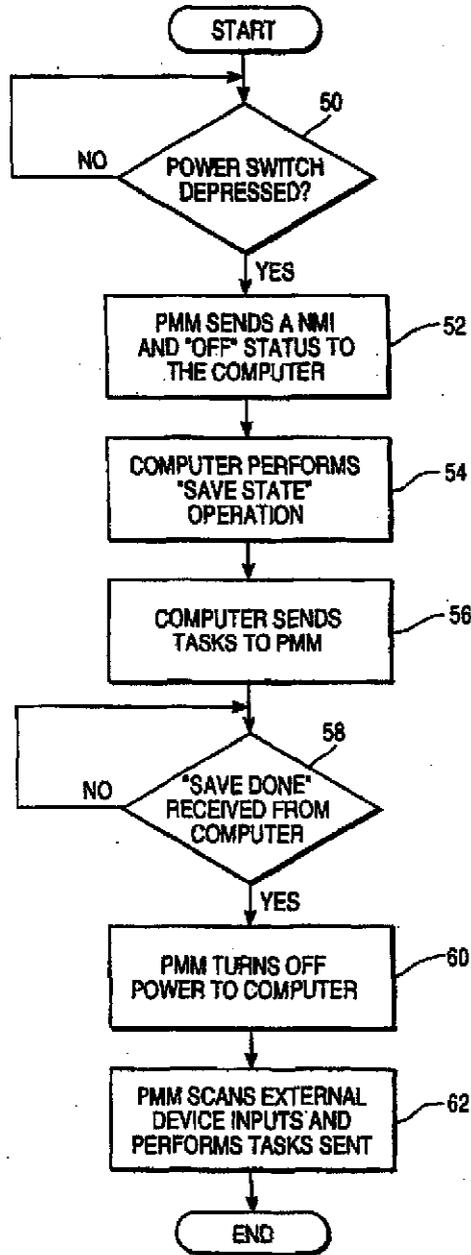


FIG. 4

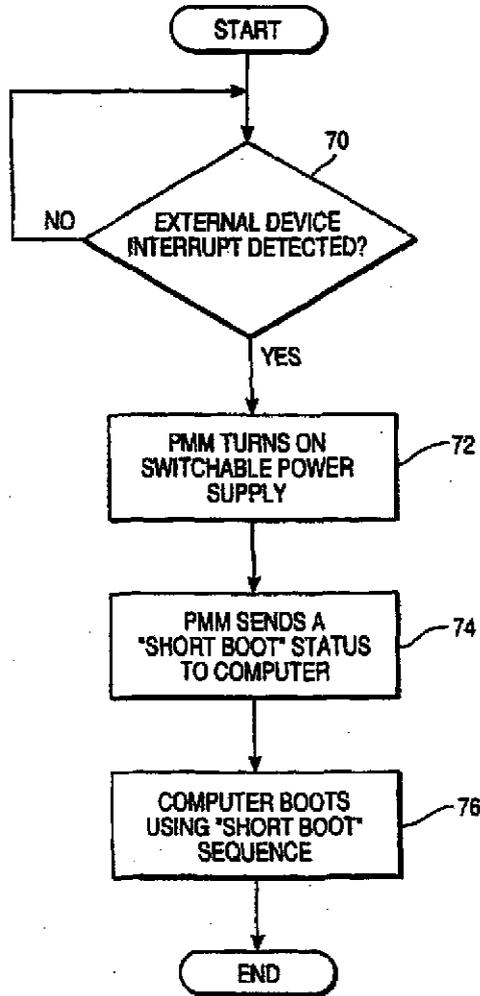


FIG. 5

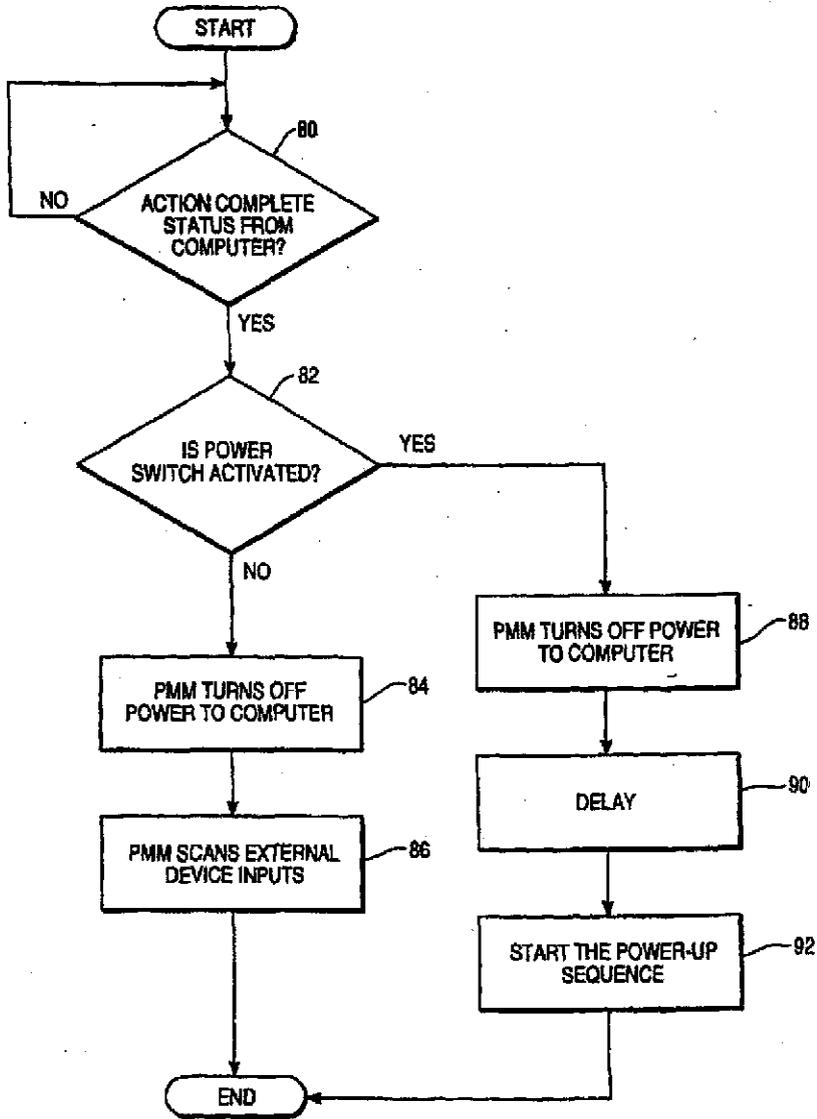


FIG. 6

## POWER-MANAGEMENT SYSTEM FOR A COMPUTER

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to power supply systems. In particular, the present invention relates to a power management system for personal computers that provides power to the computer system in response to interrupts from external devices.

#### 2. Description of Related Art

Conventional present day computer systems include a power supply that provides the power required to operate the computer system. The power supply is coupled to an AC voltage source and converts the AC voltage to a DC voltage. Typically, the power supply is coupled through a switch that is manually activated by the user and only provides power when the switch is closed. Since the switch is manual, it cannot be electronically activated to open and close to turn the computer off and on, respectively. Thus, the prior art does not provide a method for using external device interrupts or other electronic signals to control the application of power to the computer.

The prior art has attempted to reduce this shortcoming by keeping computers in the on or operational state continuously. However, such a practice wastes significant amounts of power. This practice also reduces the life of the electronic components that comprise computers. Additionally, with the advent of portable computers that have a very limited power supply, such continuous operation is not possible.

Therefore, there is a need for a system for providing power to a computer system in response to external events.

Another problem associated with power management systems of the prior art is the requirement of manually exiting all applications or programs being run on the computer before turning off the power. With most all personal computers, the user must exit the program before turning the power off, otherwise, the data used by the program will be destroyed or corrupted. Additionally, turning off the power without exiting the program even affects the operation of some programs. Thus, there is a need for a system that saves the state of the hardware and memory before turning off the power.

### SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies of the prior art by providing a power management system that allows power to be controlled by external devices. A preferred embodiment of the power management system of the present invention comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is coupled to and powered by the keep alive power supply. The keep alive power supply provides a voltage as long as it is coupled to a source. The computer is coupled to and powered by the switchable power supply. The switchable power supply can be switched on and off in response to a control signal.

In the preferred embodiment, the processor is coupled to the switchable power supply and provides the control signal that turns the switchable power supply on and off. The processor is also coupled to receive external device interrupts from a plurality of external devices. The external device interrupts are used to in-

struct the processor when to turn the switchable power supply on and off. One such device providing an interrupt may be an ordinary switch that is conventionally used to turn computers on and off. The processor is also coupled to the computer through an interface and preferably can issue non-maskable interrupts (NMI) to the central processing unit (CPU) of the computer.

The power management system of the present invention also includes a method for turning the computer on and off. The preferred method for providing power to the computer comprises the steps of: continuously providing power to the power management processor with a first power supply; monitoring external device interrupt lines coupled to the power management processor; providing power to the computer if an external device interrupt is received by sending a control signal to a second power supply coupled to power the computer; and sending a boot status command from the power management processor to the computer. The boot status command can be either a long boot command that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot command that brings the computer to an operational state in a much shorter time. The preferred method for turning the computer off comprises the steps of providing power to the power management processor with a first power source; monitoring external device interrupt lines coupled to the power management processor; signaling the computer when an external device interrupt is received; performing an operation that exits running programs and saves the hardware states of the computer on the hard disk; sending tasks from the computer to the power management processor; switching off a second power source coupled to the computer; and performing the tasks received in the sending step with the power management processor.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a preferred embodiment of a power management system of the present invention;

FIG. 2 is a block diagram of a preferred embodiment for the power supply of the present invention;

FIG. 3 is a flow chart for the preferred method for providing power with the system of the present invention;

FIG. 4 is a flow chart for the preferred method for turning off power with the system of the present invention;

FIG. 5 is a flow chart of a wake up sequence for providing power with the system of the present invention; and

FIG. 6 is a flow chart of a sleep sequence for turning off power with the system of the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, a preferred embodiment of a power management system constructed in accordance with the present invention is shown. The power management system preferably comprises a power management processor (PMM) 10 and a power supply 12. The PMM 10 electronically controls the power supplied to a host computer system 14. The power supply 12 provides power to both the PMM 10 and the computer 14. The power supply 12 receives an AC input on line 26. Line 28 couples the power supply 12 to the computer 14

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to provide the system power. The output of the power supply 12 on line 28 is controlled by an on/off control signal sent from the PMM 10 to the power supply 12 on line 18. The power supply 12 also provides continuous power to the PMM 10 on line 28.

Referring now to FIG. 2, a preferred embodiment of the power supply 12 is shown. The power supply 12 preferably comprises a switchable power supply 30 and a keep alive power supply 32. Both power supplies 30, 32 are preferably coupled to receive an AC power input on line 26. The keep alive power supply 32 is preferably a low wattage power supply that provides a 12 volt output in an exemplary embodiment. The keep alive power supply 32 continuously outputs power while an AC input is provided. In contrast, the switchable power supply 30 is electronically controllable, and may be selectively turned on an off using an enable (on/off control) signal on line 18. The switchable power supply 30 provides voltages of +3, -5, +12 and -12 at its outputs in an exemplary embodiment. For example, power supply by a custom made power supply manufactured by Hi-Power.

Referring back to FIG. 1, the coupling of the PMM 10 for receiving external device interrupts 16 on lines 22-24 is shown. The PMM 10 is preferably coupled to all hardware devices/interfaces (not shown) that can cause the computer 14 to wake up (i.e., switch power supply 30 to the on state). The external device interrupts 16 signal when the PMM 10 should apply or remove power from the computer 14. The external device interrupts 16 may be from a variety of devices that the user has granted permission to switch the computer on and off. It should be understood that all interfaces that can generate "WAKE UP" interrupts to the PMM 10 must be powered by the keep alive power supply 32. In the preferred embodiment, external device interrupts 16 are provided by a conventional manual switch for switching power on or off. In the preferred embodiment, an external device interrupt is also provided for a ring detect from a tip and ring interface (not shown) used with modems, facsimile machines and telephone answering machines. While the present invention will be discussed primarily with reference to these two types of external device interrupts, it should be understood to those skilled in the art that the PMM 10 could receive interrupts from a various external devices that need to turn the computer 14 on and off.

The PMM 10 is also coupled to the computer 14. The PMM 10 preferably sends a non-maskable interrupt (NMI) on line 25 to the computer 14 (i.e., the main Intel architecture based processor) and is also coupled to the computer 14 for sending status and command signals. The PMM 10 preferably maintains the communications protocol with the system BIOS (Basic Input Output System) of the computer 14. The PMM 10 sends the computer 14 status signals such as the short boot which indicates that the computer 14 is to be powered up to an operational state, and the long boot signal that indicates the computer 14 is to be powered up and also the configuration of the computer 14 and memory are to be tested. The PMM 10 also receives data from the computer 14. Once the computer 14 has been informed that the power will be removed, the computer 14 sends instructions to the PMM 10 indicating the functions that the PMM 10 is to perform when the computer 14 is in the sleep state (Power from switchable power supply 30 is off while power is provided to the PMM 10).

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The PMM 10 is preferably a microprocessor such as the Intel 8051. However, it should be understood that the PMM 10 can be based on any instruction set. The instruction set is not material to the invention. As briefly noted above, the PMM 10 controls the switchable power supply 30. In particular, the PMM 10 switches the power supply 30 on and off in response to external device interrupts 16 on lines 22-24. The PMM 10 preferably includes or is coupled to memory (not shown) for storing the tasks to be performed and other status information used in the operations just described. For example the PMM 10 preferably includes Random Access Memory (RAM) and Read Only Memory (ROM) to maintain communications protocol with the system BIOS of the computer 14. The PMM 10 also includes a device for keeping real time. The real time is then compared to alarm times for powering down or up the computer 14.

The power management system of the present invention also includes methods for operating the system described above. The methods use three levels of instructions or software. First, the PMM power management code details the operations performed by the PMM 10 such as sending the on/off control signal, keeping real time, and comparing real time to the alarm settings. Second, the system BIOS power management code, which is preferably incorporated into the conventional system BIOS of computer 14, provides a protocol that distinguishes "long boot" commands from "short boot" commands sent by the PMM 10. Third, the management system of the present invention includes an application level program interface definition (API) that operating systems, such as Microsoft Windows 3.0, and high based applications to invoke the services of the power management system.

Referring now to FIGS. 3-6, the preferred methods for performing the power on sequence, the power off sequence, the wake up sequence and the sleep sequence will be described. The power on sequence is shown in FIG. 3. When the computer 14 is in the off or sleep state, the preferred embodiment of the PMM 10 monitors the state of the Power ON/OFF switch in step 40, keeps real time and compares the real time to the alarm settings. The power on sequence is performed in response to an external interrupt indicating the switch (not shown) has been closed. Once a closed switch is detected, the PMM 10 turns on the main system power to the computer in step 42 by sending the on/off control signal to enable the switchable power supply 30. Then in step 44, the PMM 10 sends a power cycle status indication specifying a long boot command to the system BIOS of the computer 14 to boot to an operational state, identify the computer's system configuration and perform all memory tests. Once the computer 14 has been powered up, the API interacts with commercially available software to restore the computer 14 to the state and application the computer 14 was in prior to being powered down.

Referring now to FIG. 4, the power off sequence will be described. When the computer 14 is in the ON (active) state, the PMM 10 monitors the state of the power ON/OFF switch in step 50 for an external interrupt indicating that the switch is open. If a change of state in the power ON/OFF switch is detected, an external device interrupt is sent to the PMM 10 and the power off sequence is initiated. In step 52, the PMM 10 issues a NMI to the host computer 14. Upon receipt of the NMI in step 54, the host computer 14 initiates a "Save

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State" operation at the end of which the state of the hardware, as well as the state of the memory is saved to the a non-volatile storage media such as a hard disk. This particularly advantageous because it lets the computer 14 save the state of hardware and memory before the on/off control signal is sent to turn off power supply 30. These states stored in memory can later be used to re-boot the computer 14 in the exactly the same state it was in prior to power down. After completion of the Save State operation, the computer 14 assigns tasks to be performed by the PMM 10 during the SLEEP state of the computer 14 and then issues a Save Done status to the PMM in step 56. In step 58, the PMM 10 monitors the status line for the Save Done signal from the computer 14. Once the Save State operation is complete, the PMM 10 turns OFF the main system power by disabling the switchable power supply 30.

The present invention is particularly advantageous because it provides wake up and sleep sequences that allow application software, such as WINFAX, to be activated and used even though the computer 14 was in the SLEEP (OFF) state at the time the telephonic ring was first detected. More specifically, the present invention allows the computer 14 to detect a ring while the computer 14 is in the SLEEP (OFF) State, boot computer 14; activate the WINFAX software in less than 4 rings on the telephone line; receive the FAX from the FAX modem using WINFAX; store the FAX on the disk using WINFAX; and return the computer 14 to the SLEEP (OFF) state. The present invention will now be described with reference to the WINFAX application software and FAX applications, however, it should be understood by those skilled in the art that the present invention may be used with various other software applications that may be initiated by external device interrupts.

Referring now to FIG. 5, the wake up sequence is shown. The power management system of the present invention executes the wake up sequence when either (1) an external hardware event occurs, such as a ring is detected on the Tip & Ring Interface, or (2) an alarm event occurs when the real time kept by PMM 10 matches with the alarm time programmed by the computer 14. When the computer 14 is in the SLEEP state, the PMM 10 also monitors external device interrupts from the Ring Detect on the Tip & Ring Interface, and keeps real time and compares the current time against programmed alarm settings (Step 70). If a ring is detected, the PMM 10 switches power supply 30 on in step 72. Next, in step 74, the PMM 10 sends a short boot status signal to the computer 14. The short boot status signal indicates that the system BIOS is not to perform all the power-on diagnostics, hardware initialization, and memory tests, but in the interest of time, to directly restore the state of the computer 14 from an alternate bootable partition on the hard disk drive. This alternate (active) partition contains the applications needed to run the required functions of the system. The short boot process allow the present invention to boot, load the FAX software and be ready to receive the fax within four rings on the Tip & Ring interface. Finally in step 76, the computer boots using the short boot command.

Referring now to FIG. 6, the preferred method for returning the computer 14 to the SLEEP state is shown. Once the computer 14 is booted with the short boot command an is awake (on), the PMM 10 performs monitors the state of the Power ON/OFF switch and waits for "ACTION COMPLETE" status from the host

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computer 14 in step 80. Upon receipt of the "ACTION COMPLETE" status, the present invention tests whether the state of the Power ON/OFF switch changed in step 82. If the state of the Power ON/OFF switch has not changed, the PMM 10 turns off the main system power supply in step 84 and reverts back to the tasks normally performed during the SLEEP state in step 86. On the other hand, if the Power ON/OFF switch state had changed in step 82, then the PMM 10 turns off power supply 30 in step 88. In step 90, the preferred method provides a delay, and then the normal power on sequence described with reference to FIG. 3 is executed in step 92.

Having described the present invention with reference to specific embodiments, the above description is intended to illustrate the operation of the preferred embodiments and is not meant to limit the scope of the invention. The scope of the invention is to be delimited only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the true spirit and scope of the present invention.

What is claimed is:

1. A system for supplying power to a computer in response to interrupts from external devices, said system comprising:
  - a first power supply having an input and an output for converting an AC voltage to a DC voltage, the input coupled to a first AC voltage source to receive AC voltage;
  - a second power supply having a voltage input, a control input and an output for converting an AC voltage to a DC voltage in response to a control signal, said input coupled to said AC voltage source to receive AC voltage in parallel with said first power supply, said output coupled to supply power to the computer; and
  - a power management processor having a power input, the power input of the power management processor connected to the output of the first power supply wherein said power management processor is powered by said first power supply, an output of the power management processor connected to the control input of the second power supply wherein the output of the power management processor provides control signals to said second power supply, control inputs and outputs coupled to the computer, and interrupt inputs coupled to the external devices to receive interrupts from the external devices.
2. The system of claim 1 wherein the power management processor is a microprocessor.
3. The system of claim 1 wherein one of the external devices is a switch and wherein the second power supply supplies power when the switch is closed.
4. The system of claim 1 wherein the processor outputs long boot and short boot commands to the computer and is capable of sending an interrupt to the computer, and the computer performs different power up functions as directed by the boot command received from the power management processor.
5. The system of claim 1 wherein the power management processor includes a device for keeping time, and logic for outputting the control signal to the second power supply when the time reaches predetermined values.

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6. The system of claim 1 wherein the power management processor comprises memory for storing tasks to be performed by the power management processor.

7. A method for controlling with a power management processor the power supplied to a computer, wherein said computer can perform any of a plurality of boot processes, said method comprising the steps of:

continuously supplying power to the power management processor;

monitoring external device interrupt lines coupled to the power management processor;

if an external device interrupt is received in the power management processor, supplying power to the computer by sending a control signal from the power management processor to a switchable power supply, the switchable power supply being coupled to the computer for supplying power thereto; and

sending a boot status command from the power management processor to the computer to identify which boot process of said plurality of boot processes the computer is to perform.

8. The method of claim 7, wherein said computer has at least one identifiable configuration, and wherein said computer includes testable memory and wherein the step of sending may send one of:

a long boot command that brings the computer to an operational state, identifies the computer's configuration, and tests memory; and

a short boot command that brings the computer to an operational state.

9. The method for turning off the power provided to a computer from a first power source with a power management processor having a second power source, the computer being capable of performing a plurality of operations, including a save state operation said method comprising the steps of:

supplying power to the power management processor with the second power source;

monitoring external device interrupt lines coupled to the power management processor;

sending a signal from said power management processor to the computer when an external device interrupt is received by said power management processor;

performing said save state operation with the computer in response to said step of sending a signal;

sending tasks from the computer to the power management processor;

switching off the first power source by the power management processor; and

performing the tasks using the power management processor.

10. The method of claim 9, wherein the step of performing the save state operation includes performing while the computer is running a program, the steps of: exiting, by the computer, the program that the computer is running;

storing, by the computer a first state of a computer, hardware to a non-volatile media; and

storing, by the computer, a second state of a memory to a non-volatile media.

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## **EXHIBIT 2**

**United States Patent** [19]

[11] **Patent Number:** **5,870,613**

**White et al.**

[45] **Date of Patent:** **\*Feb. 9, 1999**

- [54] **POWER MANGEMENT SYSTEM FOR A COMPUTER**
- [75] **Inventors:** Dave White; Yen Wei Lee; Rod Ang, all of San Jose; Ray Barbieri, Campbell, all of Calif.; James Chen, Taipei, Taiwan; Suh Chluh Lee, Palo Alto, Calif.
- [73] **Assignee:** Smith Corona/Acer
- [\*] **Notice:** The term of this patent shall not extend beyond the expiration date of Pat. No. 5,410,713.

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- [21] **Appf. No.:** 422,599
- [22] **Filed:** Apr. 14, 1995

*Primary Examiner*—George B. Davis  
*Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

**Related U.S. Application Data**

- [63] Continuation of Ser. No. 816,108, Jan. 2, 1992, Pat. No. 5,410,713.
- [51] **Int. Cl.<sup>6</sup>** ..... G06F 11/00; G05B 23/02
- [52] **U.S. Cl.** ..... 395/750.01; 395/750.06; 395/750.07; 365/226; 365/229; 364/707
- [58] **Field of Search** ..... 395/750, 575, 395/750.01, 750.06, 750.07; 364/707; 307/66; 365/226, 229

[57] **ABSTRACT**

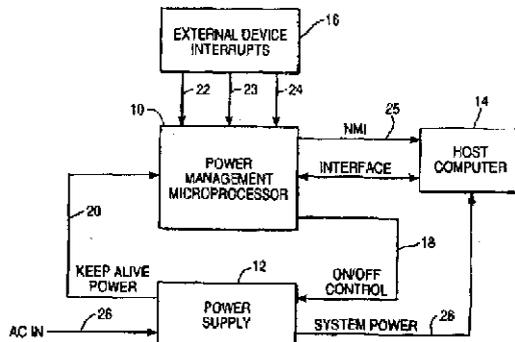
A power management system for a personal computer comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is powered by the keep alive power supply that continuously provides power. The computer is powered by a power supply that is switchable in response to a control signal. The processor preferably controls the switchable power supply. The processor is coupled to receive external device interrupts from a plurality of external devices that instruct the processor when to turn the switchable power supply on and off. The processor is also coupled to the computer through an interface. The power management system also includes a method for turning the computer on and off. A preferred method uses the processor to control the power provided to the computer. The preferred method also uses the processor to dictate whether the computer will perform a long boot that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot that brings the computer to an operational state in a much shorter time. A preferred method for turning the computer off includes the ability to exit program being run by the computer, and saving the hardware state of the computer on the hard disk.

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**13 Claims, 5 Drawing Sheets**





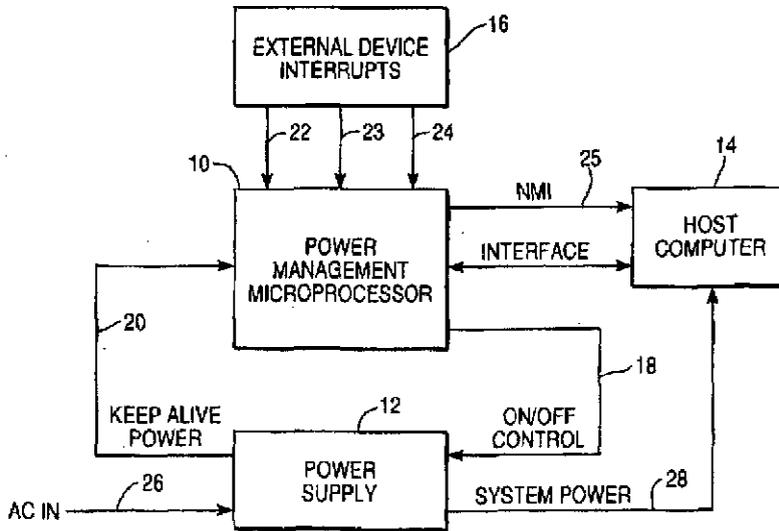


FIG. 1

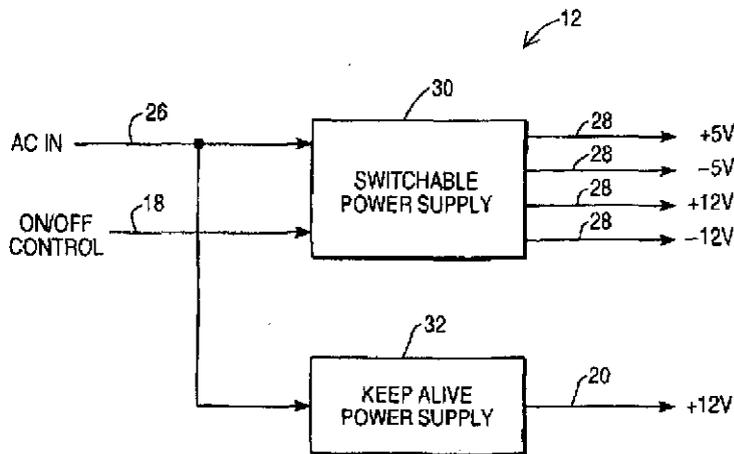


FIG. 2

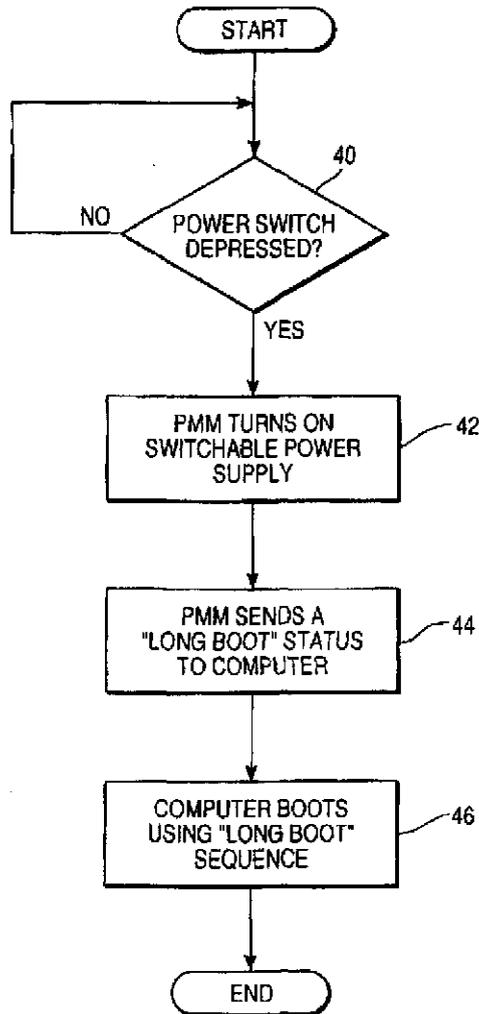


FIG. 3

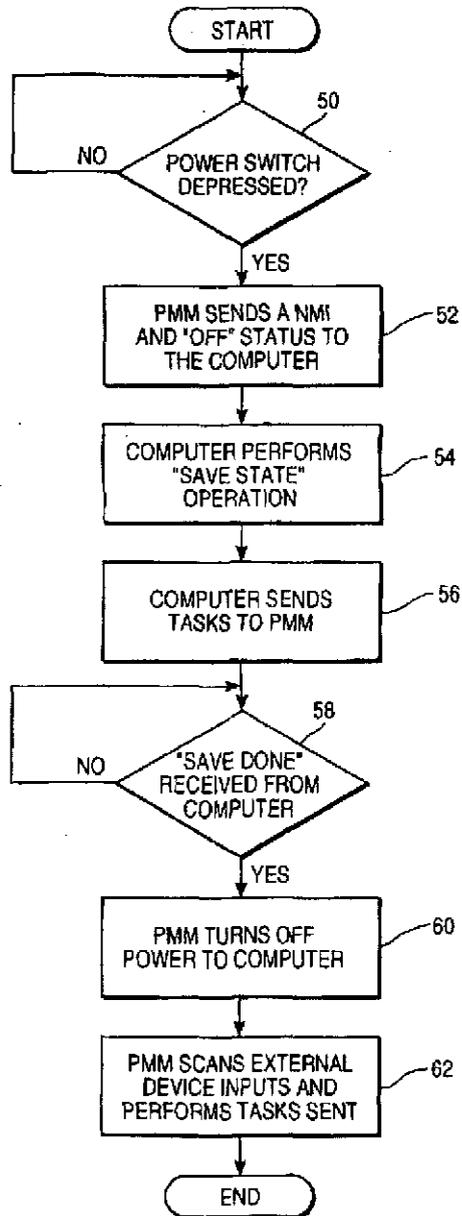


FIG. 4

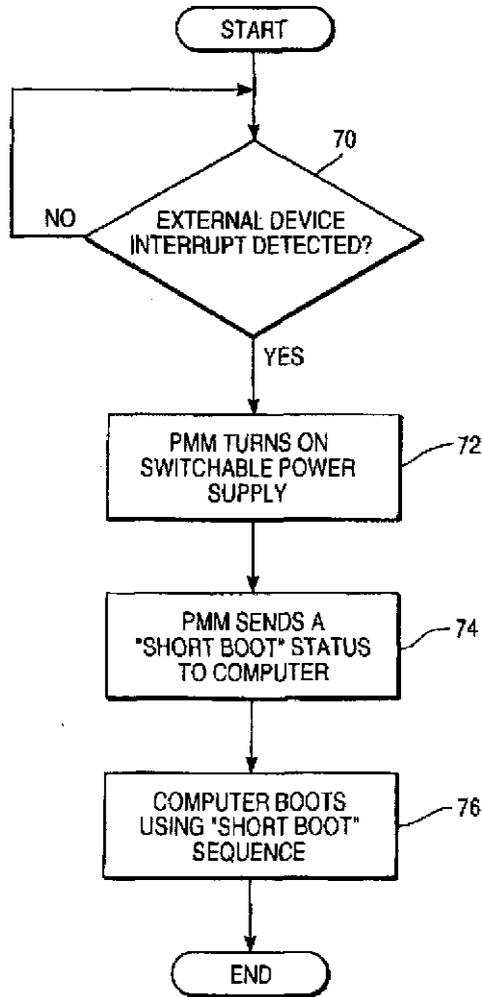


FIG. 5

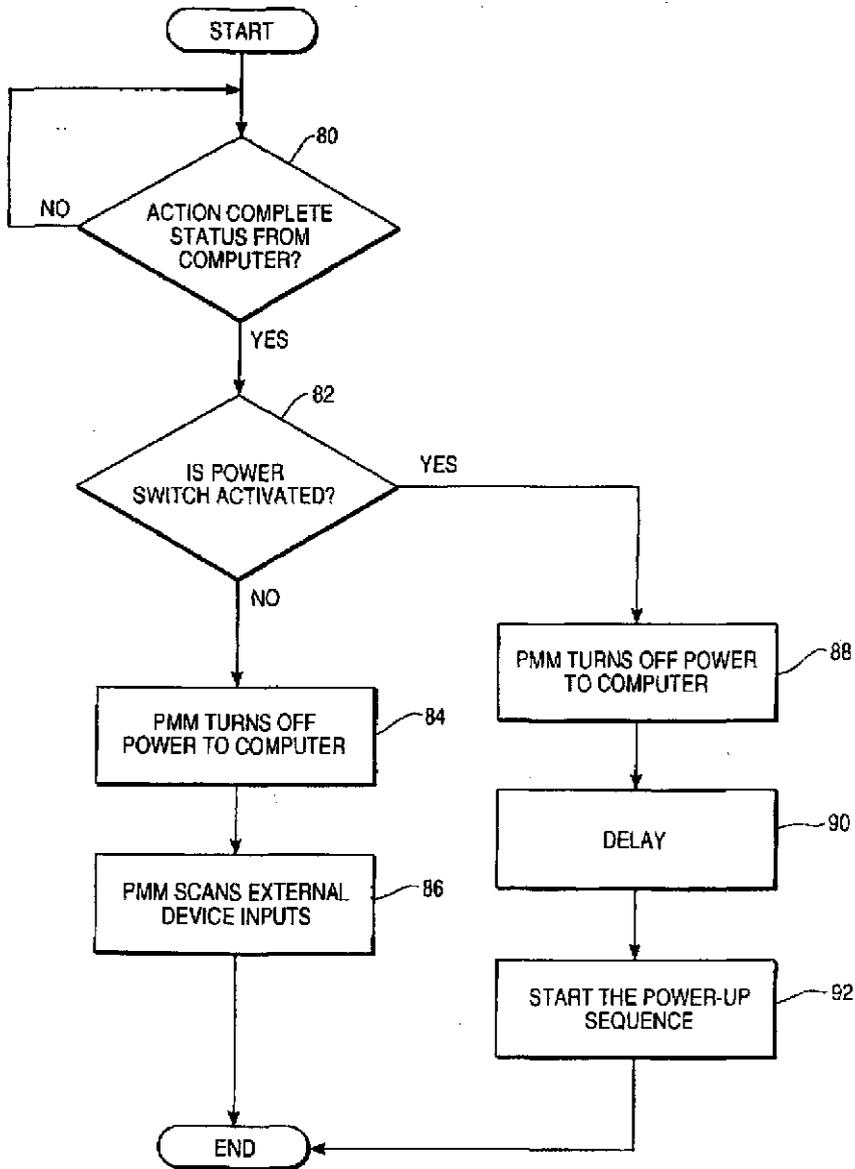


FIG. 6

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## POWER MANAGEMENT SYSTEM FOR A COMPUTER

This is a continuation of application Ser. No. 07/816,108  
filed Jan. 2, 1992, now U.S. Pat. No. 5,410,713.

### BACKGROUND OF THE INVENTION

#### 1. Field of the Invention

The present invention relates to power supply systems. In particular, the present invention relates to a power management system for personal computers that provides power to the computer system in response to interrupts from external devices.

#### 2. Description of Related Art

Conventional present day computer systems include a power supply that provides the power required to operate the computer system. The power supply is coupled to an AC voltage source and converts the AC voltage to a DC voltage. Typically, the power supply is coupled through a switch that is manually activated by the user and only provides power when the switch is closed. Since the switch is manual, it cannot be electronically activated to open and close to turn the computer off and on, respectively. Thus, the prior art does not provide a method for using external device interrupts or other electronic signals to control the application of power to the computer.

The prior art has attempted to reduce this shortcoming by keeping computers in the on or operational state continuously. However, such a practice wastes significant amounts of power. This practice also reduces the life of the electronic components that comprise computers. Additionally, with the advent of portable computers that have a very limited power supply, such continuous operation is not possible.

Therefore, there is a need for a system for providing power to a computer system in response to external events.

Another problem associated with power management systems of the prior art is the requirement of manually exiting all applications or programs being run on the computer before turning off the power. With most all personal computers, the user must exit the program before turning the power off, otherwise, the data used by the program will be destroyed or corrupted. Additionally, turning off the power without exiting the program even affects the operation of some programs. Thus, there is a need for a system that saves the state of the hardware and memory before turning off the power.

### SUMMARY OF THE INVENTION

The present invention overcomes the deficiencies of the prior art by providing a power management system that allows power to be controlled by external devices. A preferred embodiment of the power management system of the present invention comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is coupled to and powered by the keep alive power supply. The keep alive power supply provides a voltage as long as it is coupled to a source. The computer is coupled to and powered by the switchable power supply. The switchable power supply can be switched on and off in response to a control signal.

In the preferred embodiment, the processor is coupled to the switchable power supply and provides the control signal that turns the switchable power supply on and off. The processor is also coupled to receive external device interrupts from a plurality of external devices. The external

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device interrupts are used to instruct the processor when to turn the switchable power supply on and off. One such device providing an interrupt may be an ordinary switch that is conventionally used to turn computers on and off. The processor is also coupled to the computer through an interface and preferably can issue non-maskable interrupts (NMI) to the central processing unit (CPU) of the computer.

The power management system of the present invention also includes a method for turning the computer on and off. The preferred method for providing power to the computer comprises the steps of: continuously providing power to the power management processor with a first power supply; monitoring external device interrupt lines coupled to the power management processor; providing power to the computer if an external device interrupt is received by sending a control signal to a second power supply coupled to power the computer; and sending a boot status command from the power management processor to the computer. The boot status command can be either a long boot command that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot command that brings the computer to an operational state in a much shorter time. The preferred method for turning the computer off comprises the steps of providing power to the power management processor with a first power source; monitoring external device interrupt lines coupled to the power management processor; signaling the computer when an external device interrupt is received; performing an operation that exits running programs and saves the hardware states of the computer on the hard disk; sending tasks from the computer to the power management processor; switching off a second power source coupled to the computer; and performing the tasks received in the sending step with the power management processor.

### BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram of a preferred embodiment of a power management system of the present invention;

FIG. 2 is a block diagram of a preferred embodiment for the power supply of the present invention;

FIG. 3 is a flow chart for the preferred method for providing power with the system of the present invention;

FIG. 4 is a flow chart for the preferred method for turning off power with the system of the present invention;

FIG. 5 is a flow chart of a wake up sequence for providing power with the system of the present invention; and

FIG. 6 is a flow chart of a sleep sequence for turning off power with the system of the present invention.

### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Referring now to FIG. 1, a preferred embodiment of a power management system constructed in accordance with the present invention is shown. The power management system preferably comprises a power management processor (PMM) 10 and a power supply 12. The PMM 10 electronically controls the power supplied to a host computer system 14. The power supply 12 provides power to both the PMM 10 and the computer 14. The power supply 12 receives an AC input on line 26. Line 28 couples the power supply 12 to the computer 14 to provide the system power. The output of the power supply 12 on line 28 is controlled by an on/off control signal sent from the PMM 10 to the power supply 12 on line 18. The power supply 12 also provides continuous power to the PMM 10 on line 20.

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Referring now to FIG. 2, a preferred embodiment of the power supply 12 is shown. The power supply 12 preferably comprises a switchable power supply 30 and a keep alive power supply 32. Both power supplies 30, 32 are preferably coupled to receive an AC power input on line 26. The keep alive power supply 32 is preferably a low wattage power supply that provides a 12 volt output in an exemplary embodiment. The keep alive power supply 32 continuously outputs power while an AC input is provided. In contrast, the switchable power supply 30 is electronically controllable, and may be selectively turned on an off using an enable (on/off control) signal on line 18. The switchable power supply 30 provides voltages of +5, -5, +12 and -12 at its outputs in an exemplary embodiment. For example, the power supply could be a custom made power supply manufactured by Hi-Power.

Referring back to FIG. 1, the coupling of the PMM 10 for receiving external device interrupts 16 on lines 22-24 is shown. The PMM 10 is preferably coupled to all hardware devices/interfaces (not shown) that can cause the computer 14 to wake up (i.e., switch power supply 30 to the on state). The external device interrupts 16 signal when the PMM 10 should apply or remove power from the computer 14. The external device interrupts 16 may be from a variety of devices that the user has granted permission to switch the computer on and off. It should be understood that all interfaces that can generate "WAKE UP" interrupts to the PMM 10 must be powered by the keep alive power supply 32. In the preferred embodiment, external device interrupts 16 are provided by a conventional manual switch for switching power on or off. In the preferred embodiment, an external device interrupt is also provided for a ring detect from a tip and ring interface (not shown) used with modems, facsimile machines and telephone answering machines. While the present invention will be discussed primarily with reference to these two types of external device interrupts, it should be understood to those skilled in the art that the PMM 10 could receive interrupts from a various external devices that need to turn the computer 14 on and off.

The PMM 10 is also coupled to the computer 14. The PMM 10 preferably sends a non-maskable interrupt (NMI) on line 25 to the computer 14 (i.e., the main Intel architecture based processor) and is also coupled to the computer 14 for sending status and command signals. The PMM 10 preferably maintains the communications protocol with the system BIOS (Basic Input Output System) of the computer 14. The PMM 10 sends the computer 14 status signals such as the short boot which indicates that the computer 14 is to be powered up to an operational state, and the long boot signal that indicates the computer 14 is to be powered up and also the configuration of the computer 14 and memory are to be tested. The PMM 10 also receives data from the computer 14. Once the computer 14 has been informed that the power will be removed, the computer 14 sends instructions to the PMM 10 indicating the functions that the PMM 10 is to perform when the computer 14 is in the sleep state (Power from switchable power supply 30 is off while power is provided to the PMM 10).

The PMM 10 is preferably a microprocessor such as the Intel 8051. However, it should be understood that the PMM 10 can be based on any instruction set. The instruction set is not material to the invention. As briefly noted above, the PMM 10 controls the switchable power supply 30. In particular, the PMM 10 switches the power supply 30 on and off in response to external device interrupts 16 on lines 22-24. The PMM 10 preferably includes or is coupled to memory (not shown) for storing the tasks to be performed

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and other status information used in the operations just described. For example the PMM 10 preferably includes Random Access Memory (RAM) and Read Only Memory (ROM) to maintain communications protocol with the system BIOS of the computer 14. The PMM 10 also includes a device for keeping real time. The real time is then compared to alarm times for powering down or up the computer 14.

The power management system of the present invention also includes methods for operating the system described above. The methods use three levels of instructions or software. First, the PMM power management code details the operations performed by the PMM 10 such as sending the on/off control signal, keeping real time, and comparing real time to the alarm settings. Second, the system BIOS power management code, which is preferably incorporated into the conventional system BIOS of computer 14, provides to a protocol that distinguishes "long boot" commands from "short boot" commands sent by the PMM 10. Third, the management system of the present invention includes an application level program interface definition (API) that operating systems, such as Microsoft Windows 3.0, and higher based applications to invoke the services of the power management system.

Referring now to FIG. 3-6, the preferred methods for performing the power on sequence, the power off sequence, the wake up sequence and the sleep sequence will be described. The power on sequence is shown in FIG. 3. When the computer 14 is in the off or sleep state, the preferred embodiment of the PMM 10 monitors the state of the Power ON/OFF switch in step 40, keeps real time and compares the real time to the alarm settings. The power on sequence is performed in response to an external interrupt indicating the switch (not shown) has been closed. Once a closed switch is detected, the PMM 10 turns on the main system power to the computer in step 42 by sending the on/off control signal to enable the switchable power supply 30. Then in step 44, the PMM 10 sends a power cycle status indication specifying a long boot command to the system BIOS of the computer 14 to boot to an operational state, identify the computer's system configuration and perform all memory tests. Once the computer 14 has been powered up, the API interacts with commercially available software to restore the computer 14 to the state and application the computer 14 was in prior to being powered down.

Referring now to FIG. 4, the power off sequence will be described. When the computer 14 is in the ON (active) state, the PMM 10 monitors the state of the power ON/OFF switch in step 50 for an external interrupt indicating that the switch is open. If a change of state in the power ON/OFF switch is detected, an external device interrupt is sent to the PMM 10 and the power off sequence is initiated. In step 52, the PMM 10 issues a NMI to the host computer 14. Upon receipt of the NMI in step 54, the host computer 14 initiates a "Save State" operation at the end of which the state of the hardware, as well as the state of the memory is saved to a non-volatile storage media such as a hard disk. This particularly advantageous because it lets the computer 14 save the state of hardware and memory before the on/off control signal is sent to turn off power supply 30. These states stored in memory can later be used to re-boot the computer 14 in the exactly the same state it was in prior to power down. After completion of the Save State operation, the computer 14 assigns tasks to be performed by the PMM 10 during the SLEEP state of the computer 14 and then issues a Save Done status to the PMM in step 56. In step 58, the PMM 10 monitors the status line for the Save Done signal from the computer 14. Once the Save State operation is complete, the PMM 10

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turns OFF the main system power by disabling the switchable power supply 30.

The present invention is particularly advantageous because it provides wake up and sleep sequences that allow application software, such as WINFAX, to be activated and used even though the computer 14 was in the SLEEP (OFF) state at the time the telephone ring was first detected. More specifically, the present invention allows the computer 14 to detect a ring while the computer 14 is in the SLEEP (OFF) State; boot computer 14; activate the WINFAX software in less than 4 rings on the telephone line; receive the FAX from the FAX modem using WINFAX; store the FAX on the disk using WINFAX; and return the computer 14 to the SLEEP (OFF) state. The present invention will now be described with reference to the WINFAX application software and FAX applications, however, it should be understood by those skilled in the art that the present invention may be used with various other software applications that may be initiated by external device interrupts.

Referring now to FIG. 5, the wake up sequence is shown. The power management system of the present invention executes the wake up sequence when either (1) an external hardware event occurs, such as a ring is detected on the Tip & Ring Interface, or (2) an alarm event occurs when the real time kept by PMM 10 matches with the alarm time programmed by the computer 14. When the computer 14 is in the SLEEP state, the PMM 10 also monitors external device interrupts 16 from the Ring Detect on the Tip & Ring Interface, and keeps real time and compares the current time against programmed alarm settings (Step 70). If a ring is detected, the PMM 10 switches power supply 30 on in step 72. Next, in step 74, the PMM 10 sends a short boot status signal to the computer 14. The short boot status signal indicates that the system BIOS is not to perform all the power-on diagnostics, hardware initialization, and memory tests, but in the interest of time, to directly restore the state of the computer 14 from an alternate bootable partition on the hard disk drive. This alternate (active) partition contains the applications needed to run the required functions of the system. The short boot process allows the present invention to boot, load the FAX software and be ready to receive the fax within four rings on the Tip & Ring interface. Finally in step 76, the computer boots using the short boot command.

Referring now to FIG. 6, the preferred method for returning the computer 14 to the SLEEP state is shown. Once the computer 14 is booted with the short boot command and is awake (on), the PMM 10 monitors the state of the Power ON/OFF switch and waits for "ACTION COMPLETE" status from the host computer 14 in step 80. Upon receipt of the "ACTION COMPLETE" status, the present invention tests whether the state of the Power ON/OFF switch has changed in step 82. If the state of the Power ON/OFF switch has not changed, the PMM 10 turns off the main system power supply in step 84 and reverts back to the tasks normally performed during the SLEEP state in step 86. On the other hand, if the Power ON/OFF switch state had changed in step 82, then the PMM 10 turns off power supply 30 in step 88. In step 90, the preferred method provides a delay, and then the normal power on sequence described with reference to FIG. 3 is executed in step 92.

Having described the present invention with reference to specific embodiments, the above description is intended to illustrate the operation of the preferred embodiments and is not meant to limit the scope of the invention. The scope of the invention is to be delimited only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the true spirit and scope of the present invention.

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What is claimed is:

1. A system for supplying power to a computer in response to interrupts from external devices, the system comprising:
  - a first power supply having an input and an output for converting an AC voltage to a DC voltage, the input coupled to a first AC voltage source to receive AC voltage;
  - a second power supply having a voltage input, a control input, and an output for converting an AC voltage to a DC voltage in response to a control signal, the input coupled to the AC voltage source to receive AC voltage in parallel with the first power supply, the output coupled to supply power to the computer; and
  - a power management circuit having a power input, the power input of the power management circuit coupled to the output of the first power supply wherein the power management circuit is powered by the first power supply, an output of the power management circuit coupled to the control input of the second power supply wherein the output of the power management circuit provides control signals to the second power supply, control inputs and outputs coupled to the computer, and interrupt inputs coupled to the external devices to receive interrupts from the external devices.
2. The system of claim 1 wherein one of the external devices is a tip & ring interface.
3. The system of claim 1 wherein one of the external devices is a switch and wherein the second power supply supplies power when the switch is closed.
4. The system of claim 1 wherein the power management circuit outputs long boot and short boot commands to the computer and is capable of sending an interrupt to the computer, and the computer performs different power up functions as directed by the boot command received from the power management circuit.
5. The system of claim 1 wherein the power management circuit includes a device for keeping time, and logic for outputting the control signal to the second power supply when the time reaches predetermined values.
6. The system of claim 1 wherein the power management circuit comprises memory for storing tasks to be performed by the power management circuit.
7. A system for supplying power to a computer in response to interrupts from external devices, the system comprising:
  - a first power supply having an input and an output for converting an AC voltage to a DC voltage, the input coupled to a first AC voltage source to receive AC voltage;
  - a second power supply having a voltage input, a control input, and an output for converting an AC voltage to a DC voltage in response to a control signal, the input coupled to the AC voltage source to receive AC voltage in parallel with the first power supply, the output coupled to supply power to the computer; and
  - power management means, powered by the first power supply and coupled to the computer, for providing the control signal to the second power supply in response to interrupts from the external devices.
8. The system of claim 7 wherein one of the external devices is a tip & ring interface.
9. The system of claim 7 wherein one of the external devices is a switch and the second power supply supplies power when the switch is closed.

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10. The system of claim 7 wherein:  
the power management means includes means for out-  
putting long boot and short boot commands to the  
computer, and means for sending an interrupt to the  
computer; and

the computer performs different power up functions as  
directed by the boot command received from the power  
management means.

11. The system of claim 7 wherein the power management  
means includes means for keeping time, and means for  
outputting the control signal to the second power supply  
when the time reaches predetermined values.

12. The system of claim 7 wherein the power management  
means includes means for storing tasks to be performed by  
the power management means.

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13. A system for supplying power to a computer in  
response to interrupts from external devices, the system  
comprising:

a first power supply;

a second power supply that is coupled to the computer and  
is switchable in response to a control signal;

means, powered by the first power supply, for monitoring  
external device interrupt lines; and

means, powered by the first power supply and responsive  
to an external device interrupt being received, for  
sending the control signal to the second power supply,  
thereby causing the second power supply to supply  
power to the computer.

\* \* \* \* \*

# **EXHIBIT 3**

US005903765A

**United States Patent** [19]

[11] **Patent Number:** **5,903,765**

**White et al.**

[45] **Date of Patent:** **May 11, 1999**

- [54] **POWER MANAGEMENT SYSTEM FOR A COMPUTER**
- [75] **Inventors:** **Dave White; Yen Wei Lee; Rod Ang,** all of San Jose; **Ray Barbieri,** Campbell, all of Calif.; **James Chen,** Taipei, Taiwan; **Suh Chhueh Lee,** Palo Alto, Calif.
- [73] **Assignee:** **Smith Corona/Acer**
- [21] **Appl. No.:** **08/825,663**
- [22] **Filed:** **Apr. 3, 1997**

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**Related U.S. Application Data**

- [62] Division of application No. 08/422,599, Apr. 14, 1995, Pat. No. 5,870,613, which is a continuation of application No. 07/816,108, Jan. 2, 1992, Pat. No. 5,410,713.
- [51] **Int. Cl.<sup>o</sup>** ..... **G06F 1/26; G06F 1/32**
- [52] **U.S. CL.** ..... **395/750.02**
- [58] **Field of Search** ..... **395/750.02, 750.01, 395/750.03, 750.05; 364/707**

*Primary Examiner*—Robert W. Dowos  
*Attorney, Agent, or Firm*—Townsend and Townsend and Crew LLP

**ABSTRACT**

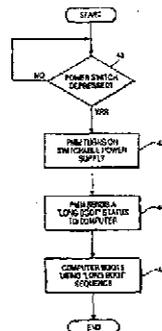
[57] A power management system for a personal computer comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is powered by the keep alive power supply that continuously provides power. The computer is powered by a power supply that is switchable in response to a control signal. The processor preferably controls the switchable power supply. The processor is coupled to receive external device interrupts from a plurality of external devices that instruct the processor when to turn the switchable power supply on and off. The processor is also coupled to the computer through an interface. The power management system also includes a method for turning the computer on and off. A preferred method uses the processor to control the power provided to the computer. The preferred method also uses the processor to dictate whether the computer will perform a long boot that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot that brings the computer to an operational state in a much shorter time. A preferred method for turning the computer off includes the ability to exit program being run by the computer, and saving the hardware state of the computer on the hard disk.

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**15 Claims, 5 Drawing Sheets**



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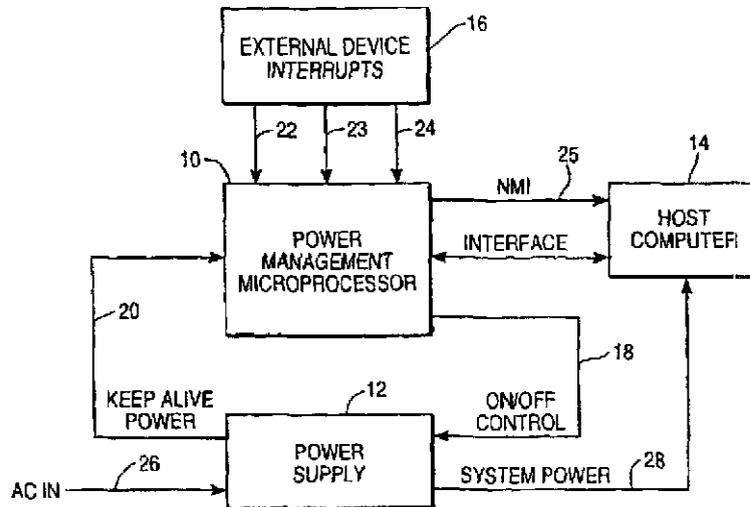


FIG. 1

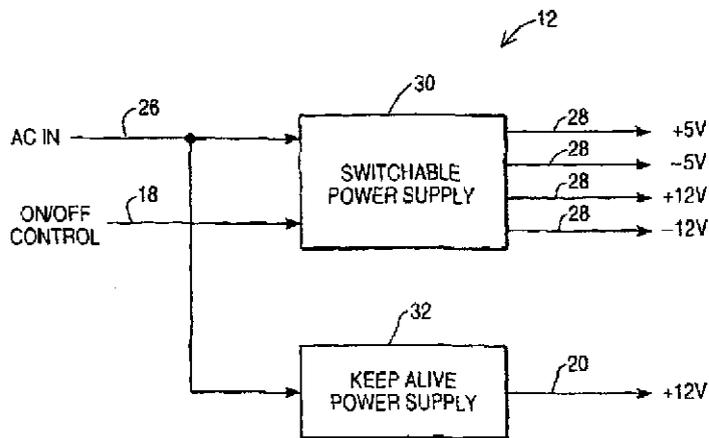


FIG. 2

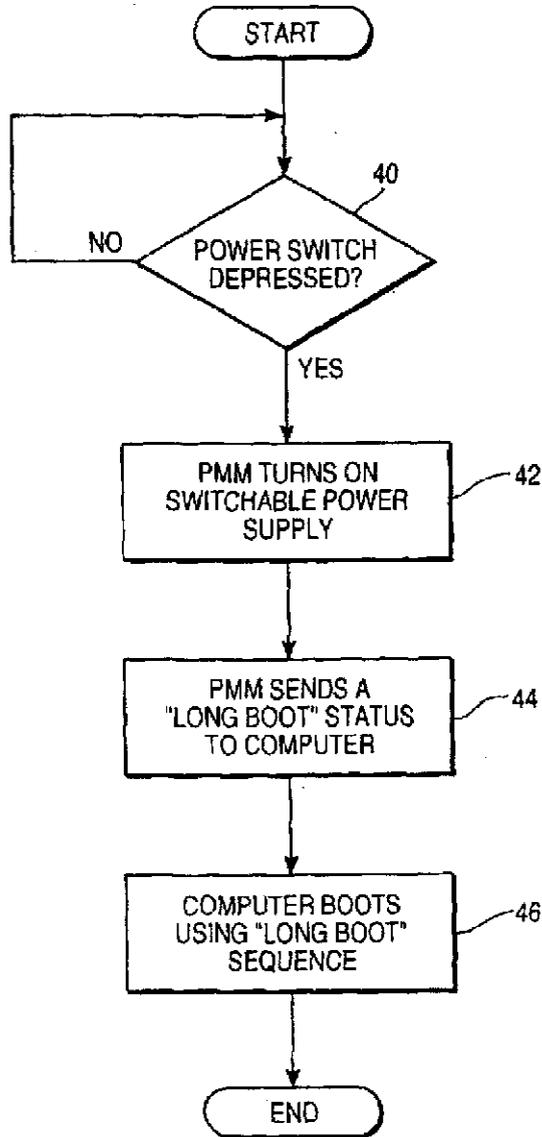


FIG. 3

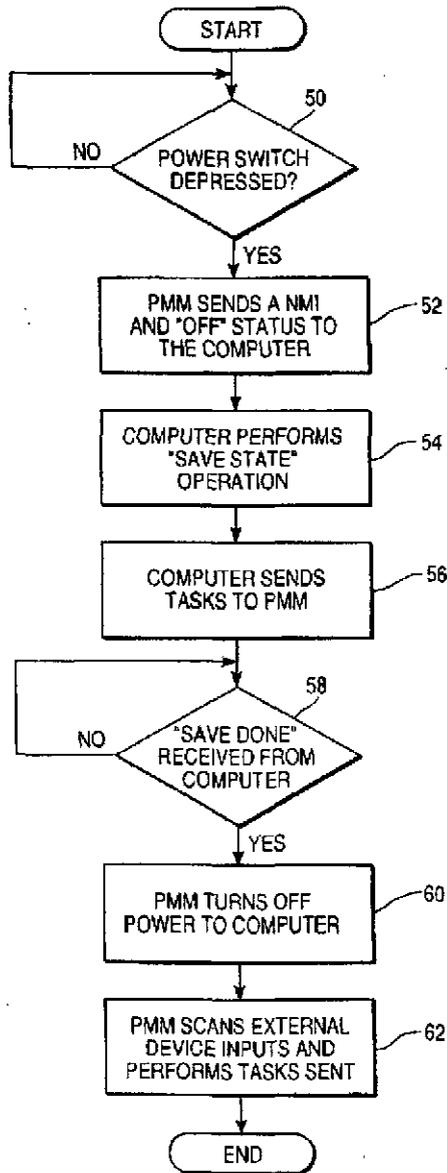


FIG. 4

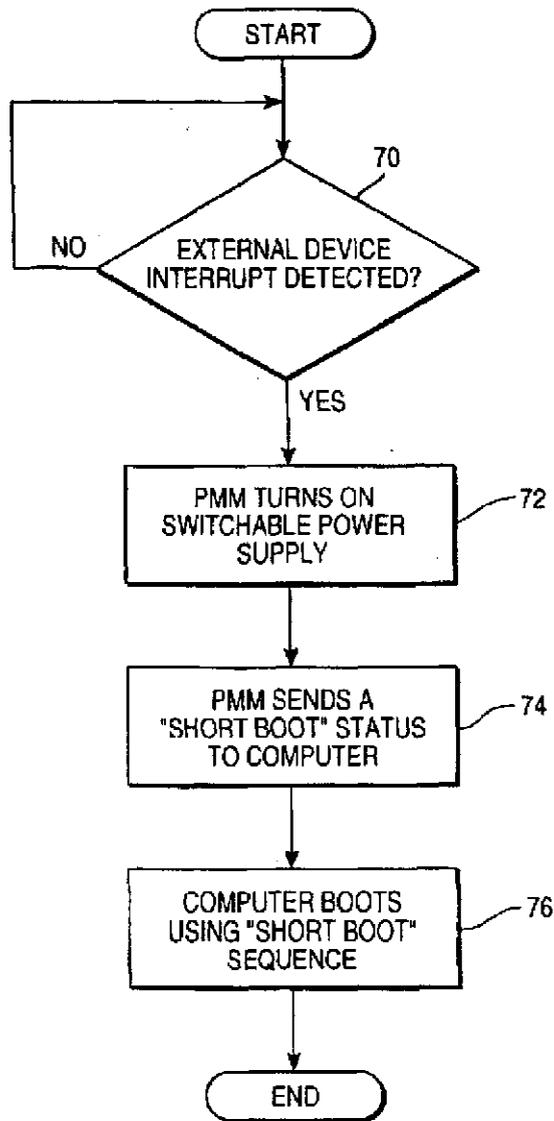


FIG. 5

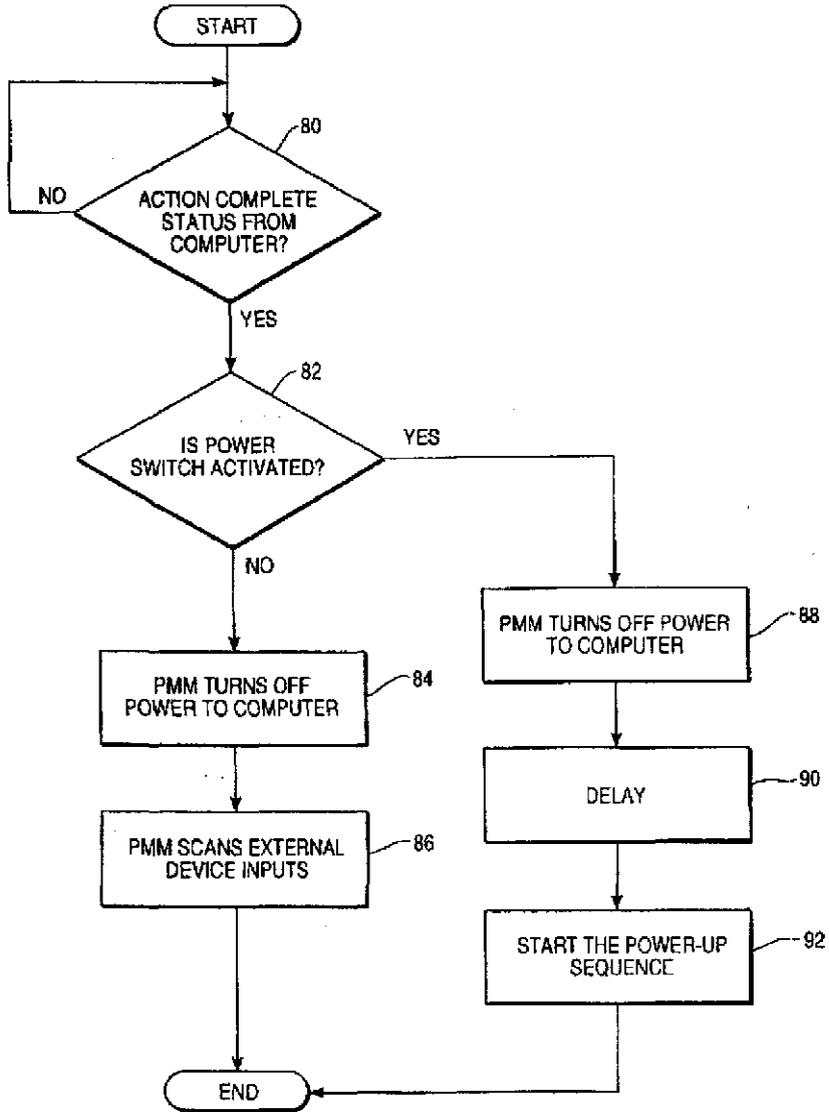


FIG. 6

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**1**  
**POWER MANAGEMENT SYSTEM FOR A  
 COMPUTER**

This is a Division of application Ser. No. 08/422,599, filed Apr. 14, 1995, now U.S. Pat. No. 5,870,613, issued Feb. 9, 1989, which is a continuation of application Ser. No. 07/816,108, filed Jan. 2, 1992, now U.S. Pat. No. 5,410,713, issued Apr. 25, 1995, the disclosure of which is incorporated by reference.

**BACKGROUND OF THE INVENTION**

**1. Field of the Invention**

The present invention relates to power supply systems. In particular, the present invention relates to a power management system for personal computers that provides power to the computer system in response to interrupts from external devices.

**2. Description of Related Art**

Conventional present day computer systems include a power supply that provides the power required to operate the computer system. The power supply is coupled to an AC voltage source and converts the AC voltage to a DC voltage. Typically, the power supply is coupled through a switch that is manually activated by the user and only provides power when the switch is closed. Since the switch is manual, it cannot be electronically activated to open and close to turn the computer off and on, respectively. Thus, the prior art does not provide a method for using external device interrupts or other electronic signals to control the application of power to the computer.

The prior art has attempted to reduce this shortcoming by keeping computers in the on or operational state continuously. However, such a practice wastes significant amounts of power. This practice also reduces the life of the electronic components that comprise computers. Additionally, with the advent of portable computers that have a very limited power supply, such continuous operation is not possible.

Therefore, there is a need for a system for providing power to a computer system in response to external events.

Another problem associated with power management systems of the prior art is the requirement of manually exiting all applications or programs being run on the computer before turning off the power. With most all personal computers, the user must exit the program before turning the power off, otherwise, the data used by the program will be destroyed or corrupted. Additionally, turning off the power without exiting the program even affects the operation of some programs. Thus, there is a need for a system that saves the state of the hardware and memory before turning off the power.

**SUMMARY OF THE INVENTION**

The present invention overcomes the deficiencies of the prior art by providing a power management system that allows power to be controlled by external devices. A preferred embodiment of the power management system of the present invention comprises a power management processor, a switchable power supply and a keep alive power supply. The processor is coupled to and powered by the keep alive power supply. The keep alive power supply provides a voltage as long as it is coupled to a source. The computer is coupled to and powered by the switchable power supply. The switchable power supply can be switched on and off in response to a control signal.

In the preferred embodiment, the processor is coupled to the switchable power supply and provides the control signal

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that turns the switchable power supply on and off. The processor is also coupled to receive external device interrupts from a plurality of external devices. The external device interrupts are used to instruct the processor when to turn the switchable power supply on and off. One such device providing an interrupt may be an ordinary switch that is conventionally used to turn computers on and off. The processor is also coupled to the computer through an interface and preferably can issue non-maskable interrupts (NMI) to the central processing unit (CPU) of the computer.

The power management system of the present invention also includes a method for turning the computer on and off. The preferred method for providing power to the computer comprises the steps of: continuously providing power to the power management processor with a first power supply; monitoring external device interrupt lines coupled to the power management processor; providing power to the computer if an external device interrupt is received by sending a control signal to a second power supply coupled to power the computer; and sending a boot status command from the power management processor to the computer. The boot status command can be either a long boot command that brings the computer to an operational state, identifies the computer's configuration, and tests memory, or a short boot command that brings the computer to an operational state in a much shorter time. The preferred method for turning the computer off comprises the steps of providing power to the power management processor with a first power source; monitoring external device interrupt lines coupled to the power management processor; signaling the computer when an external device interrupt is received; performing an operation that exits running programs and saves the hardware states of the computer on the hard disk; sending tasks from the computer to the power management processor; switching off a second power source coupled to the computer; and performing the tasks received in the sending step with the power management processor.

**BRIEF DESCRIPTION OF THE DRAWINGS**

FIG. 1 is a block diagram of a preferred embodiment of a power management system of the present invention;

FIG. 2 is a block diagram of a preferred embodiment for the power supply of the present invention;

FIG. 3 is a flow chart for the preferred method for providing power with the system of the present invention;

FIG. 4 is a flow chart for the preferred method for turning off power with the system of the present invention;

FIG. 5 is a flow chart of a wake up sequence for providing power with the system of the present invention; and

FIG. 6 is a flow chart of a sleep sequence for turning off power with the system of the present invention.

**DETAILED DESCRIPTION OF THE  
 PREFERRED EMBODIMENTS**

Referring now to FIG. 1, a preferred embodiment of a power management system constructed in accordance with the present invention is shown. The power management system preferably comprises a power management processor (PMM) 10 and a power supply 12. The PMM 10 electronically controls the power supplied to a host computer system 14. The power supply 12 provides power to both the PMM 10 and the computer 14. The power supply 12 receives an AC input on line 26. Line 28 couples the power supply 12 to the computer 14 to provide the system power. The output of the power supply 12 on line 28 is

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controlled by an on/off control signal sent from the PMM 10 to the power supply 12 on line 18. The power supply 12 also provides continuous power to the PMM 10 on line 20.

Referring now to FIG. 2, a preferred embodiment of the power supply 12 is shown. The power supply 12 preferably comprises a switchable power supply 30 and a keep alive power supply 32. Both power supplies 30, 32 are preferably coupled to receive an AC power input on line 26. The keep alive power supply 32 is preferably a low wattage power supply that provides a 12 volt output in an exemplary embodiment. The keep alive power supply 32 continuously outputs power while an AC input is provided. In contrast, the switchable power supply 30 is electronically controllable, and may be selectively turned on an off using an enable (on/off control) signal on line 18. The switchable power supply 30 provides voltages of +5, -5, +12 and -12 at its outputs in an exemplary embodiment. For example, the power supply could be a custom made power supply manufactured by Hi-Power.

Referring back to FIG. 1, the coupling of the PMM 10 for receiving external device interrupts 16 on lines 22-24 is shown. The PMM 10 is preferably coupled to all hardware devices/interfaces (not shown) that can cause the computer 14 to wake up (i.e., switch power supply 30 to the on state). The external device interrupts 16 signal when the PMM 10 should apply or remove power from the computer 14. The external device interrupts 16 may be from a variety of devices that the user has granted permission to switch the computer on and off. It should be understood that all interfaces that can generate "WAKE UP" interrupts to the PMM 10 must be powered by the keep alive power supply 32. In the preferred embodiment, external device interrupts 16 are provided by a conventional manual switch for switching power on or off. In the preferred embodiment, an external device interrupt is also provided for a ring detect from a tip and ring interface (not shown) used with modems, facsimile machines and telephone answering machines. While the present invention will be discussed primarily with reference to these two types of external device interrupts, it should be understood to those skilled in the art that the PMM 10 could receive interrupts from a various external devices that need to turn the computer 14 on and off.

The PMM 10 is also coupled to the computer 14. The PAM 10 preferably sends a non-maskable interrupt (NMI) on line 25 to the computer 14 (i.e., the main Intel architecture based processor) and is also coupled to the computer 14 for sending status and command signals. The PMM 10 preferably maintains the communications protocol with the system BIOS (Basic Input Output System) of the computer 14. The PMM 10 sends the computer 14 status signals such as the short boot which indicates that the computer 14 is to be powered up to an operational state, and the long boot signal that indicates the computer 14 is to be powered up and also the configuration of the computer 14 and memory are to be tested. The PMM 10 also receives data from the computer 14. Once the computer 14 has been informed that the power will be removed, the computer 14 sends instructions to the PAM 10 indicating the functions that the PMM 10 is to perform when the computer 14 is in the sleep state (Power from switchable power supply 30 is off while power is provided to the PMM 10).

The PMM 10 is preferably a microprocessor such as the Intel 8051. However, it should be understood that the PMM 10 can be based on any instruction set. The instruction set is not material to the invention. As briefly noted above, the PMM 10 controls the switchable power supply 30. In particular, the PMM 10 switches the power supply 30 on and

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off in response to external device interrupts 16 on lines 22-24. The PMM 10 preferably includes or is coupled to memory (not shown) for storing the tasks to be performed and other status information used in the operations just described. For example the PMM 10 preferably includes Random Access Memory (RAM) and Read Only Memory (ROM) to maintain communications protocol with the system BIOS of the computer 14. The PMM 10 also includes a device for keeping real time. The real time is then compared to alarm times for powering down or up the computer 14.

The power management system of the present invention also includes methods for operating the system described above. The methods use three levels of instructions or software. First, the PMM power management code details the operations performed by the PMM 10 such as sending the on/off control signal, keeping real time, and comparing real time to the alarm settings. Second, the system BIOS power management code, which is preferably incorporated into the conventional system BIOS of computer 14, provides to a protocol that distinguishes "long boot" commands from "short boot" commands sent by the PMM 10. Third, the management system of the present invention includes an application level program interface definition (API) that operating systems, such as Microsoft Windows 3.0, and higher based applications to invoke the services of the power management system.

Referring now to FIGS. 3-6, the preferred methods for performing the power on sequence, the power off sequence, the wake up sequence and the sleep sequence will be described. The power on sequence is shown in FIG. 3. When the computer 14 is in the off or sleep state, the preferred embodiment of the PMM 10 monitors the state of the Power ON/OFF switch in step 40, keeps real time and compares the real time to the alarm settings. The power on sequence is performed in response to an external interrupt indicating the switch (not shown) has been closed. Once a closed switch is detected, the PMM 10 turns on the main system power to the computer in step 42 by sending the on/off control signal to enable the switchable power supply 30. Then in step 44, the PMM 10 sends a power cycle status indication specifying a long boot command to the system BIOS of the computer 14 to boot to an operational state, identify the computer's system configuration and perform all memory tests. Once the computer 14 has been powered up, the API interacts with commercially available software to restore the computer 14 to the state and application the computer 14 was in prior to being powered down.

Referring now to FIG. 4, the power off sequence will be described. When the computer 14 is in the ON (active) state, the PMM 10 monitors the state of the power ON/OFF switch in step 50 for an external interrupt indicating that the switch is open. If a change of state in the power ON/OFF switch is detected, an external device interrupt is sent to the PMM 10 and the power off sequence is initiated. In step 52, the PMM 10 issues a NMI to the host computer 14. Upon receipt of the NMI in step 54, the host computer 14 initiates a "Save State" operation at the end of which the state of the hardware, as well as the state of the memory is saved to a non-volatile storage media such as a hard disk. This particularly advantageous because it lets the computer 14 save the state of hardware and memory before the on/off control signal is sent to turn off power supply 30. These states stored in memory can later be used to re-boot the computer 14 in the exactly the same state it was in prior to power down. After completion of the Save State operation, the computer 14 assigns tasks to be performed by the PMM 10 during the SLEEP state of the computer 14 and then issues a Save Done status

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to the PMM in step 56. In step 58, the PMM 10 monitors the status line for the Save Done signal from the computer 14. Once the Save State operation is complete, the PMM 10 turns OFF the main system power by disabling the switchable power supply 30.

The present invention is particular advantageous because it provides wake up and sleep sequences that allow application software, such as WINFAX, to be activated and used even though the computer 14 was in the SLEEP (OFF) state at the time the telephone ring was first detected. More specifically, the present invention allows the computer 14 to detect a ring while the computer 14 is in the SLEEP (OFF) State, boot computer 14; activate the WINFAX software in less than 4 rings on the telephone line; receive the FAX from the FAX modem using WINFAX; store the FAX on the disk using WINFAX; and return the computer 14 to the SLEEP (OFF) state. The present invention will now be described with reference to the WINFAX application software and FAX applications, however, it should be understood by those skilled in the art that the present invention may be used with various other software applications that may be initiated by external device interrupts.

Referring now to FIG. 5, the wake up sequence is shown. The power management system of the present invention executes the wake up sequence when either (1) an external hardware event occurs, such as a ring is detected on the Tip & Ring Interface, or (2) an alarm event occurs when the real time kept by PMM 10 matches with the alarm time programmed by the computer 14. When the computer 14 is in the SLEEP state, the PAM 10 also monitors external device interrupts 16 from the Ring Detect on the Tip & Ring Interface, and keeps real time and compares the current time against programmed alarm settings (Step 70). If a ring is detected, the PMM 10 switches power supply 30 on in step 72. Next, in step 74, the PMM 10 sends a short boot status signal to the computer 14. The short boot status signal indicates that the system BIOS is not to perform all the power-on diagnostics, hardware initialization, and memory tests, but in the interest of time, to directly restore the state of the computer 14 from an alternate bootable partition on the hard disk drive. This alternate (active) partition contains the applications needed to run the required functions of the system. The short boot process allows the present invention to boot, load the FAX software and be ready to receive the fax within four rings on the Tip & Ring interface. Finally in step 76, the computer boots using the short boot command.

Referring now to FIG. 6, the preferred method for returning the computer 14 to the SLEEP state is shown. Once the computer 14 is booted with the short boot command an is awake (on), the PMM 10 monitors the state of the Power ON/OFF switch and waits for "ACTION COMPLETE" status from the host computer 14 in step 80. Upon receipt of the "ACTION COMPLETE" status, the present invention tests whether the state of the Power ON/OFF switch has changed in step 82. If the state of the Power ON/OFF switch has not changed, the PMM 10 turns off the main system power supply in step 84 and reverts back to the tasks normally performed during the SLEEP state in step 86. On the other hand, if the Power ON/OFF switch state had changed in step 82, then the PMM 10 turns off power supply 30 in step 88. In step 90, the preferred method provides a delay, and then the normal power on sequence described with reference to FIG. 3 is executed in step 92.

Having described the present invention with reference to specific embodiments, the above description is intended to illustrate its operation of the preferred embodiments and is not meant to limit the scope of the invention. The scope of

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the invention is to be defined only by the following claims. From the above discussion, many variations will be apparent to one skilled in the art that would yet be encompassed by the true spirit and scope of the present invention.

What is claimed is:

1. A method of controlling power supplied to a computer, wherein the computer can perform any of a plurality of boot processes, the method comprising:

monitoring external device interrupt lines during a period in which power is not supplied to the computer;

if an external device interrupt is received during the period, supplying power to the computer by sending a control signal to a switchable power supply, the switchable power supply being coupled to the computer for supplying power thereto;

sending boot status command to the computer to identify which boot process of the plurality of distinct boot processes the computer is to perform; and

booting up the computer in accordance with the identified boot process.

2. The method of claim 1, wherein the computer has at least one identifiable configuration, and wherein the computer includes testable memory and wherein the sending of the boot status command may send one of:

a long boot command that brings the computer to an operational state, identifies the computer's configuration, and tests memory; and

a short boot command that brings the computer to an operational state, without identifying the computer's configuration or testing memory.

3. The method of claim 1 wherein the external device interrupt is generated by a switch.

4. A method for turning off power provided to a computer from a power source, the computer being capable of performing a plurality of operations, including a save state operation, the method comprising:

sending a signal to the computer upon receipt of an external device interrupt;

performing the save state operation with the computer in response to the sending of the signal;

specifying, by the computer, tasks to be performed while the power source of the computer is switched off, wherein the tasks include a plurality of operations in accordance with a stored code;

switching of the power source of the computer; and performing the specified tasks after switching off the power source of the computer.

5. The method of claim 4, wherein the performing the save state operation includes performing, while the computer is running a program:

exiting, by the computer, the program that the computer is running;

storing, by the computer, a first state of a computer hardware to a non-volatile media; and

storing, by the computer, a second state of a memory to a non-volatile media.

6. The method of claim 4 wherein each of the plurality of operations is selected from a group comprising:

sending a control signal;

keeping real time; and

comparing real time to a preset time.

7. The method of claim 4 wherein the external device interrupt is generated by a switch.

8. A method of waking up a computer to execute an application in response to an event, the method comprising:

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restoring power to the computer in response to the event,  
the computer being in a powered off state immediately  
before the event occurs;  
sending a boot status signal to the computer, the boot  
status signal identifying which one of a plurality of  
distinct boot processes the computer is to perform;  
booting the computer in accordance with the identified  
boot process;  
loading the application into a main memory of the com-  
puter; and  
executing the application on the computer.  
9. The method of claim 8, wherein the event occurs when  
a current time equals a programmed time.  
10. The method of claim 8, wherein the event occurs upon  
receipt of an external device interrupt.  
11. The method of claim 10, wherein the external device  
interrupt is a ring detected on a tip and ring interface.  
12. The method of claim 11, wherein the application is a  
FAX application.  
13. The method of claim 10 wherein the external device  
interrupt is generated by a switch.

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14. The method of claim 8, wherein the boot status signal  
is a short boot status signal that causes the computer to not  
perform power-on diagnostics, hardware initialization, and  
memory tests while booting but rather to perform a state  
restoration from an alternative bootable partition on a hard  
disk drive of the computer, the partition containing the  
application.  
15. The method of claim 8, further comprising:  
generating in the computer a signal indicating that execu-  
tion of the application has completed;  
determining if a switch controlling power to the computer  
has been activated;  
turning off power to the computer; and  
if the switch has been activated, turning on power to the  
computer after a delay from when the power to the  
computer is turned off; and  
sending a long boot status signal to the computer.

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